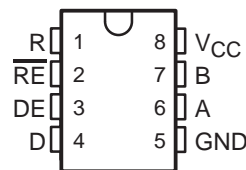


# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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- Meet or Exceed the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27
- Operate at Data Rates up to 35 MBaud
- Four Skew Limits Available:
  - SN65ALS176 . . . 15 ns
  - SN75ALS176 . . . 10 ns
  - SN75ALS176A . . . 7.5 ns
  - SN75ALS176B . . . 5 ns
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply-Current Requirements . . . 30 mA Max
- Wide Positive and Negative Input/Output Bus-Voltage Ranges
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Hysteresis
- Glitch-Free Power-Up and Power-Down Protection
- Receiver Open-Circuit Fail-Safe Design

D OR P PACKAGE  
(TOP VIEW)



## description

The SN65ALS176 and SN75ALS176 series differential bus transceivers are designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27.

The SN65ALS176 and SN75ALS176 series combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC} = 0$ . This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The SN65ALS176 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , and the SN75ALS176 series is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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## AVAILABLE OPTIONS

T <sub>A</sub>	t <sub>sk(lim)</sub> <sup>†</sup>	PACKAGED DEVICES	
		SMALL OUTLINE (D) <sup>‡</sup>	PLASTIC DIP (P)
0°C to 70°C	10	SN75ALS176D	SN75ALS176P
	7.5	SN75ALS176AD	SN75ALS176AP
	5	SN75ALS176BD	SN75ALS176BP
-40°C to 85°C	15	SN65ALS176D	SN65ALS176P

<sup>†</sup> t<sub>sk(lim)</sub> This is the maximum range that the driver or receiver delay times vary over temperature, V<sub>CC</sub>, and process (device to device).

<sup>‡</sup> The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN75ALS176DR).

## Function Tables

### DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

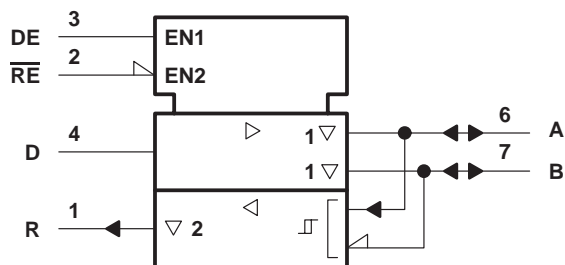
H = high level, L = low level, X = irrelevant,  
Z = high impedance

### RECEIVER

DIFFERENTIAL INPUTS A-B	ENABLE $\overline{RE}$	OUTPUT R
V <sub>ID</sub> ≥ 0.2 V	L	H
-0.2 V < V <sub>ID</sub> < 0.2 V	L	?
V <sub>ID</sub> ≤ -0.2 V	L	L
X	H	Z
Inputs open	L	H

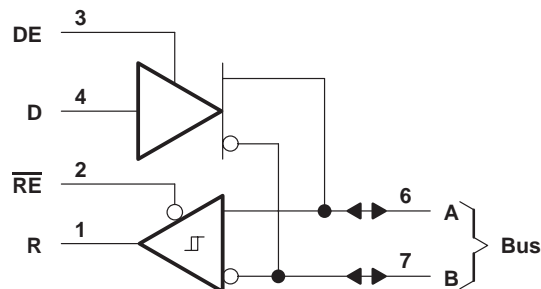
H = high level, L = low level, X = irrelevant,  
Z = high impedance

## logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

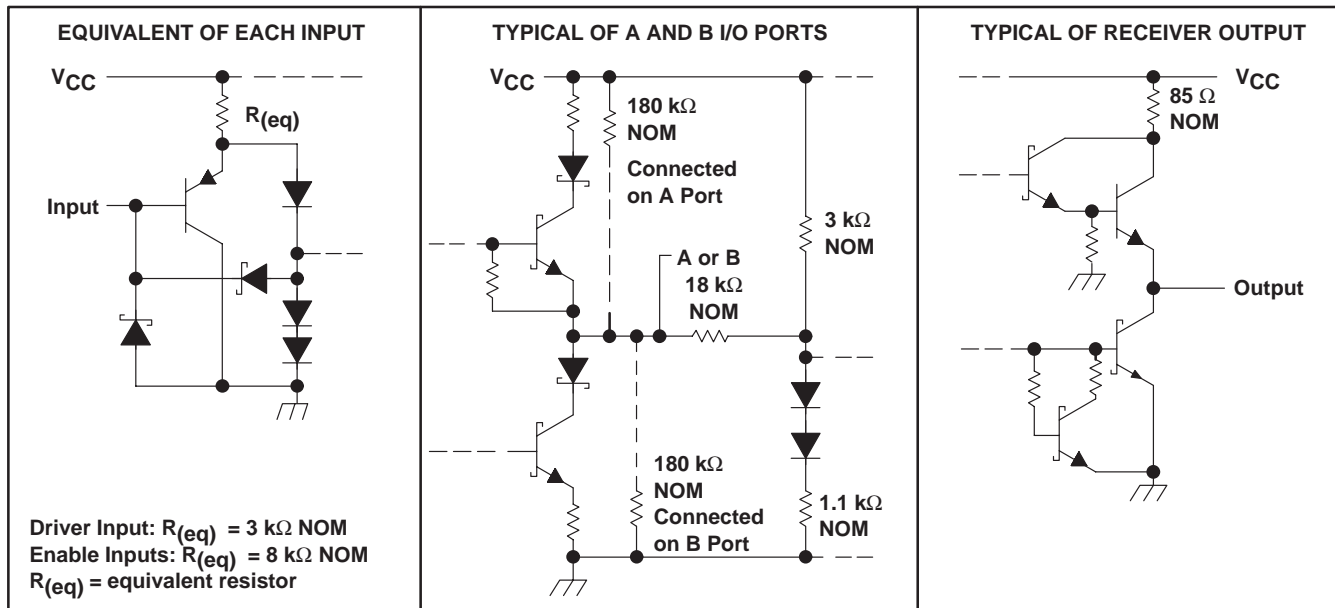
## logic diagram (positive logic)



# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Voltage range at any bus terminal	-7 V to 12 V
Enable input voltage, $V_I$	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	197°C/W
P package	104°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, $T_{Stg}$	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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## recommended operating conditions (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Input voltage at any bus terminal (separately or common mode), $V_I$ or $V_{IC}$		12			V
		-7			
High-level input voltage, $V_{IH}$	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, $V_{IL}$	D, DE, and $\overline{RE}$	0.8			V
Differential input voltage, $V_{ID}$ (see Note 3)		$\pm 12$			V
High-level output current, $I_{OH}$	Driver	-60			mA
	Receiver	-400			$\mu$ A
Low-level output current, $I_{OL}$	Driver	60			mA
	Receiver	8			
Operating free-air temperature, $T_A$	SN65ALS176	-40			$^{\circ}$ C
	SN75ALS176 series	0	70		

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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## DRIVER SECTION

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{IK}$	Input clamp voltage	$I_I = -18 \text{ mA}$				-1.5	V
$V_O$	Output voltage	$I_O = 0$		0		6	V
$ V_{OD1} $	Differential output voltage	$I_O = 0$		1.5		6	V
$ V_{OD2} $	Differential output voltage	$R_L = 100 \Omega$ ,	See Figure 1	$1/2 V_{OD1}$ or $2\text{V}^{\S}$			V
		$R_L = 54 \Omega$ ,	See Figure 1	1.5	2.5	5	V
$V_{OD3}$	Differential output voltage	$V_{test} = -7 \text{ V to } 12 \text{ V}$ ,	See Figure 2	1.5		5	V
$\Delta V_{OD} $	Change in magnitude of differential output voltage¶	$R_L = 54 \Omega \text{ or } 100 \Omega$ , See Figure 1				$\pm 0.2$	V
$V_{OC}$	Common-mode output voltage					3 -1	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage¶					$\pm 0.2$	V
$I_O$	Output current	Outputs disabled, See Note 4	$V_O = 12 \text{ V}$			1	mA
			$V_O = -7 \text{ V}$			-0.8	
$I_{IH}$	High-level input current	$V_I = 2.4 \text{ V}$				20	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0.4 \text{ V}$				-400	$\mu\text{A}$
$I_{OS}$	Short-circuit output current#	$V_O = -4 \text{ V}$	SN65ALS176			-250	mA
		$V_O = -6 \text{ V}$	SN75ALS176				
		$V_O = 0$				-150	
		$V_O = V_{CC}$				250	
		$V_O = 8 \text{ V}$					
$I_{CC}$	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

§ The minimum  $V_{OD2}$  with a 100- $\Omega$  load is either  $1/2 V_{OD1}$  or 2 V, whichever is greater.

¶  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from one logic state to the other.

# Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B

## DIFFERENTIAL BUS TRANSCEIVERS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

### SN65ALS176

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$t_d(\text{OD})$	Differential output delay time	$R_L = 54 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 3			15	ns
$t_{\text{sk}}(\text{p})$	Pulse skew‡	$R_L = 54 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 3		0	2	ns
$t_{\text{sk}}(\text{lim})$	Pulse skew§					15		
$t_t(\text{OD})$	Differential output transition time	$R_L = 54 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 3		8		ns
$t_{\text{PZH}}$	Output enable time to high level	$R_L = 110 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 4			80	ns
$t_{\text{PZL}}$	Output enable time to low level	$R_L = 110 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 5			30	ns
$t_{\text{PHZ}}$	Output disable time from high level	$R_L = 110 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 4			50	ns
$t_{\text{PLZ}}$	Output disable time from low level	$R_L = 110 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 5			30	ns

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Pulse skew is defined as the  $|t_{\text{PLH}} - t_{\text{PHL}}|$  of each channel of the same device.

§ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

### SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT	
$t_d(\text{OD})$	Differential output delay time	'ALS176	$R_L = 54 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 3	3	8	13	ns
		'ALS176A				4	7	11.5	
		'ALS176B				5	8	10	
$t_{\text{sk}}(\text{p})$	Pulse skew‡	$R_L = 54 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 3		0	2	ns	
$t_{\text{sk}}(\text{lim})$	Pulse skew§	'ALS176	$R_L = 54 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 3			10	ns
		'ALS176A						7.5	
		'ALS176B						5	
$t_t(\text{OD})$	Differential output transition time	$R_L = 54 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 3		8		ns	
$t_{\text{PZH}}$	Output enable time to high level	$R_L = 110 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 4		23	50	ns	
$t_{\text{PZL}}$	Output enable time to low level	$R_L = 110 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 5		14	20	ns	
$t_{\text{PHZ}}$	Output disable time from high level	$R_L = 110 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 4		20	35	ns	
$t_{\text{PLZ}}$	Output disable time from low level	$R_L = 110 \Omega$ ,	$C_L = 50 \text{ pF}$ ,	See Figure 5		8	17	ns	

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Pulse skew is defined as the  $|t_{\text{PLH}} - t_{\text{PHL}}|$  of each channel of the same device.

§ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

### SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
$V_O$	$V_{Oa}, V_{Ob}$	$V_{Oa}, V_{Ob}$
$ V_{OD1} $	$V_O$	$V_O$
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $	None	$V_t$ (test termination measurement 2)
$\Delta  V_{OD} $	$  V_t  -  \bar{V}_t  $	$  V_t  -  \bar{V}_t  $
$V_{OC}$	$ V_{Os} $	$ V_{Os} $
$\Delta  V_{OC} $	$ V_{Os} - \bar{V}_{Os} $	$ V_{Os} - \bar{V}_{Os} $
$I_{OS}$	$ I_{sa} ,  I_{sb} $	None
$I_O$	$ I_{xa} ,  I_{xb} $	$I_{ia}, I_{ib}$



# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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## RECEIVER SECTION

**electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>O</sub> = 2.7 V,	I <sub>O</sub> = -0.4 mA			0.2	V
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>O</sub> = 0.5 V,	I <sub>O</sub> = 8 mA	-0.2‡			V
V <sub>hys</sub>	Hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )				60		mV
V <sub>IK</sub>	Enable-input clamp voltage	I <sub>I</sub> = -18 mA				-1.5	V
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 200 mV, See Figure 6	I <sub>OH</sub> = -400 μA,		2.7		V
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -200 mV, See Figure 6	I <sub>OL</sub> = 8 mA,			0.45	V
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = 0.4 V to 2.4 V				±20	μA
V <sub>I</sub>	Line input current	Other input = 0 V, See Note 4	V <sub>I</sub> = 12 V			1	mA
			V <sub>I</sub> = -7 V			-0.8	
I <sub>IH</sub>	High-level-enable input current	V <sub>IH</sub> = 2.7 V				20	μA
I <sub>IL</sub>	Low-level-enable input current	V <sub>IL</sub> = 0.4 V				-100	μA
r <sub>I</sub>	Input resistance			12	20		kΩ
I <sub>OS</sub>	Short-circuit output current	V <sub>ID</sub> = 200 mV,	V <sub>O</sub> = 0	-15		-85	mA
I <sub>CC</sub>	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)**

### SN65ALS176

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t <sub>pd</sub>	Propagation time	V <sub>ID</sub> = -1.5 V to 1.5 V, See Figure 7	C <sub>L</sub> = 15 pF,			25	ns
t <sub>sk(p)</sub>	Pulse skew§				0	2	ns
t <sub>sk(lim)</sub>	Pulse skew¶	R <sub>L</sub> = 54 Ω, See Figure 3	C <sub>L</sub> = 50 pF,			15	ns
t <sub>PZH</sub>	Output enable time to high level	C <sub>L</sub> = 15 pF,	See Figure 8		11	18	ns
t <sub>PZL</sub>	Output enable time to low level				11	18	ns
t <sub>PHZ</sub>	Output disable time from high level					50	ns
t <sub>PLZ</sub>	Output disable time from low level					30	ns

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Pulse skew is defined as the |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

¶ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.



# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (continued)

## SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT		
t <sub>pd</sub>	Propagation time	'ALS176	V <sub>ID</sub> = -1.5 V to 1.5 V, See Figure 7	C <sub>L</sub> = 15 pF,	9	14	19	ns
		'ALS176A			10.5	14	18	
		'ALS176B			11.5	13	16.5	
t <sub>sk(p)</sub>	Pulse skew‡				0	2	ns	
t <sub>sk(lim)</sub>	Pulse skew§	'ALS176	R <sub>L</sub> = 54 Ω, See Figure 3	C <sub>L</sub> = 50 pF,		10		ns
		'ALS176A				7.5		
		'ALS176B				5		
t <sub>pZH</sub>	Output enable time to high level	C <sub>L</sub> = 15 pF, See Figure 8			7	14	ns	
t <sub>pZL</sub>	Output enable time to low level				20	35	ns	
t <sub>pHZ</sub>	Output disable time from high level				20	35	ns	
t <sub>pLZ</sub>	Output disable time from low level				8	17	ns	

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Pulse skew is defined as the |t<sub>pLH</sub> - t<sub>pHL</sub>| of each channel of the same device.

§ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

## PARAMETER MEASUREMENT INFORMATION

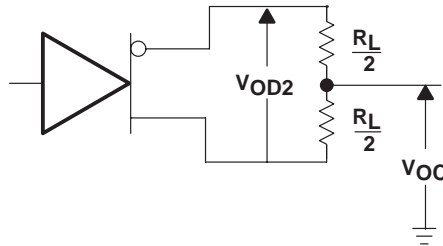


Figure 1. Driver V<sub>OD2</sub> and V<sub>OC</sub>

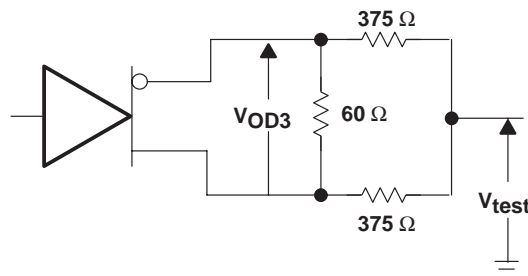
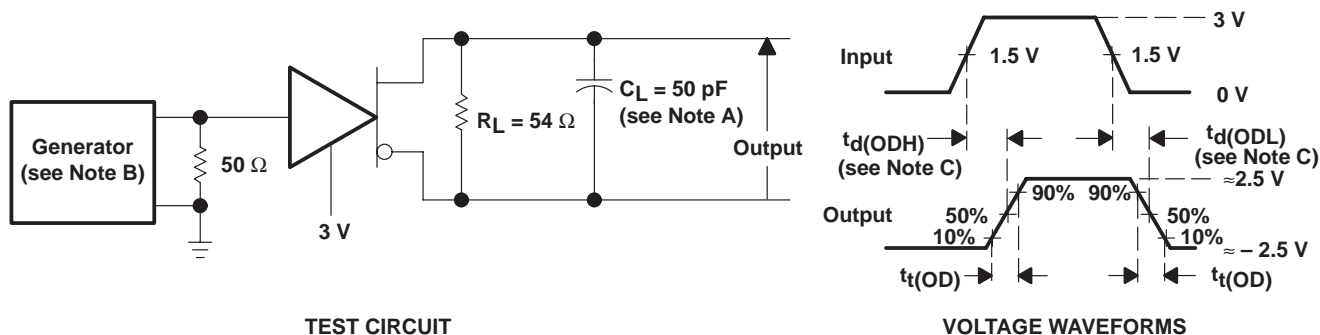


Figure 2. Driver V<sub>OD3</sub>

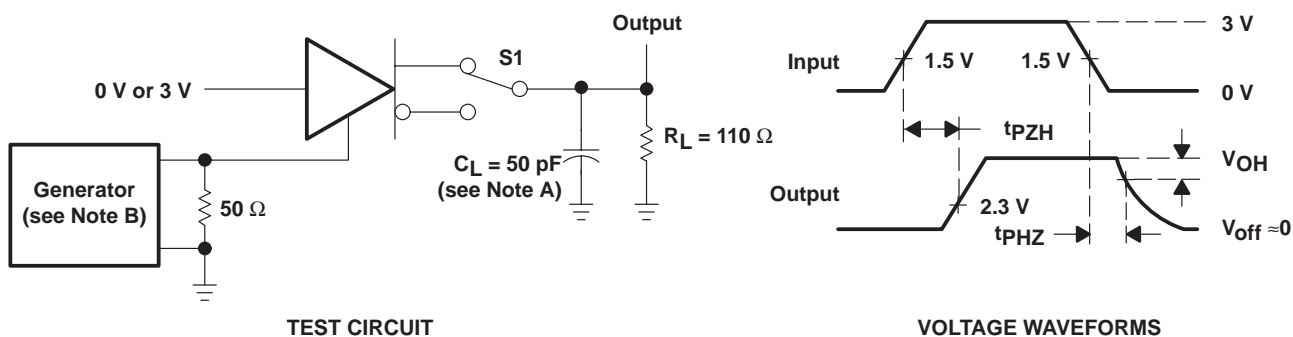


PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O = 50 \Omega$ .  
 C.  $t_d(OD) = t_d(ODH)$  or  $t_d(ODL)$

Figure 3. Driver Test Circuit and Voltage Waveforms



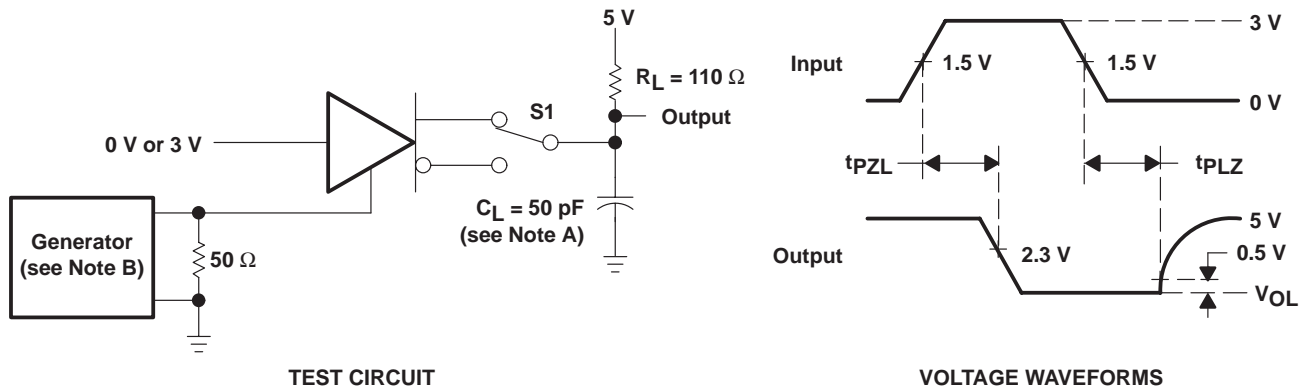
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O = 50 \Omega$ .

Figure 4. Driver Test Circuit and Voltage Waveforms

# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

Figure 5. Driver Test Circuit and Voltage Waveforms

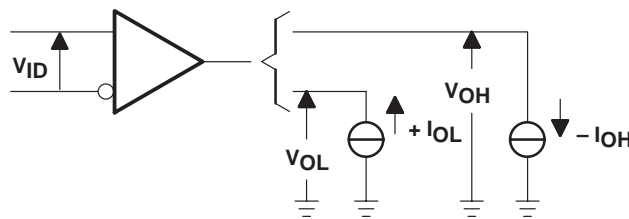
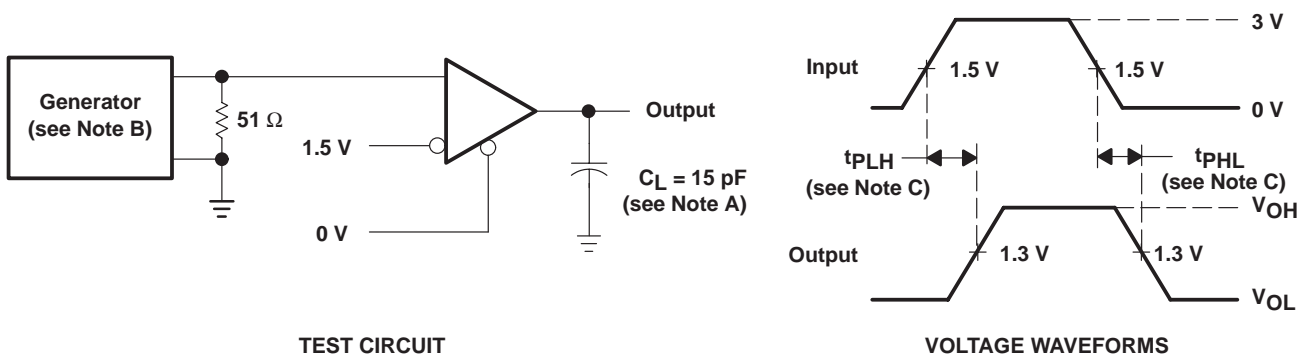


Figure 6. Receiver  $V_{OH}$  and  $V_{OL}$  Test Circuit



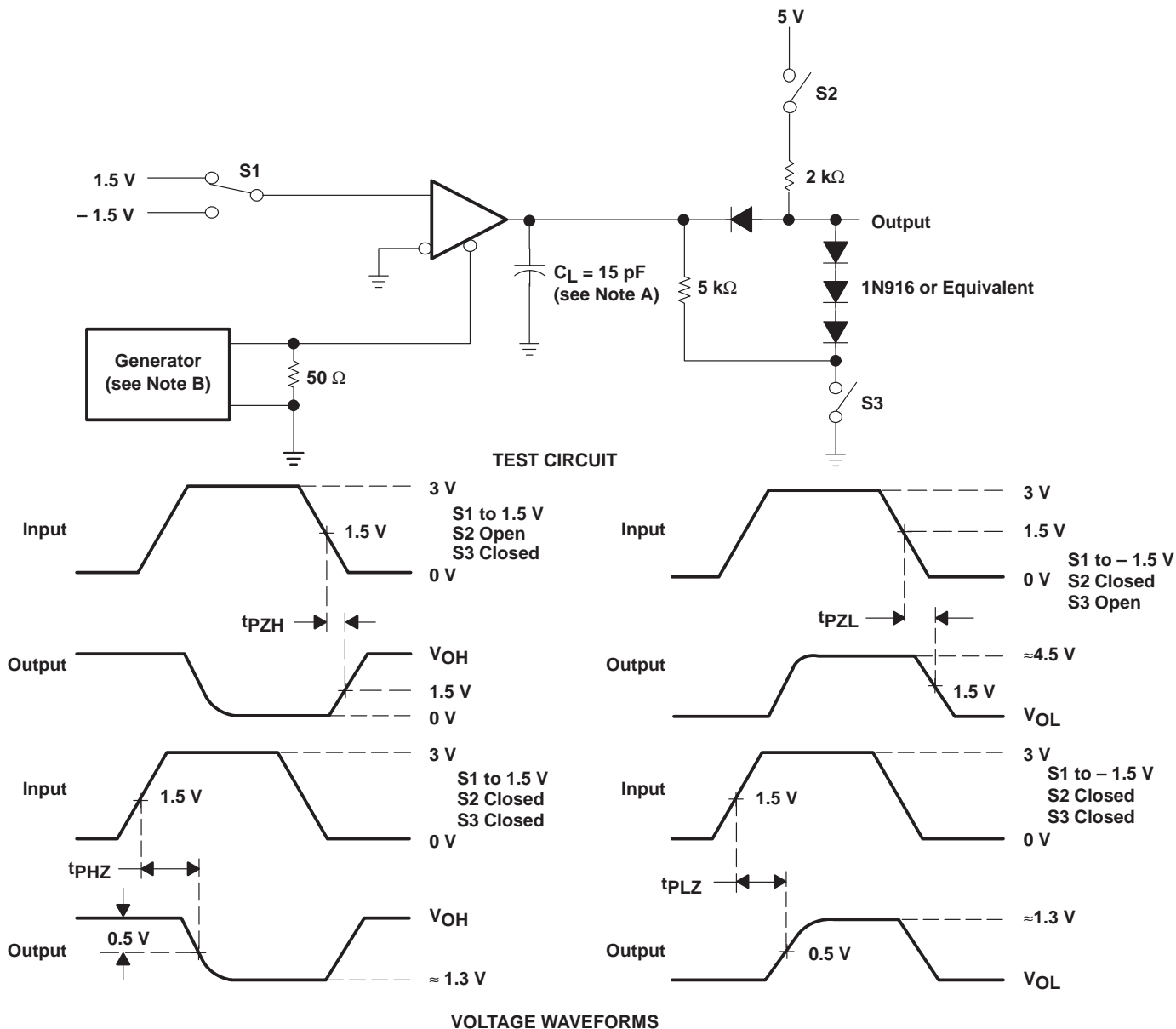
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 C.  $t_{pd} = t_{PLH}$  or  $t_{PHL}$

Figure 7. Receiver Test Circuit and Voltage Waveforms

# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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## PARAMETER MEASUREMENT INFORMATION



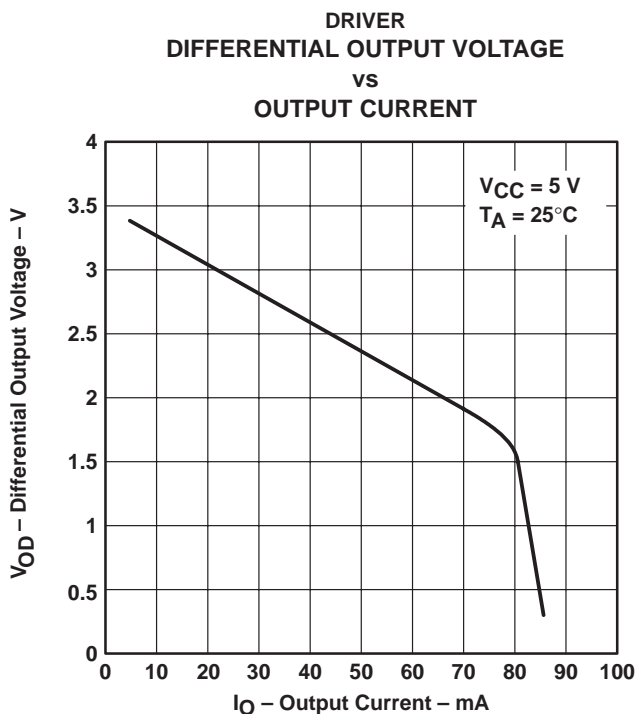
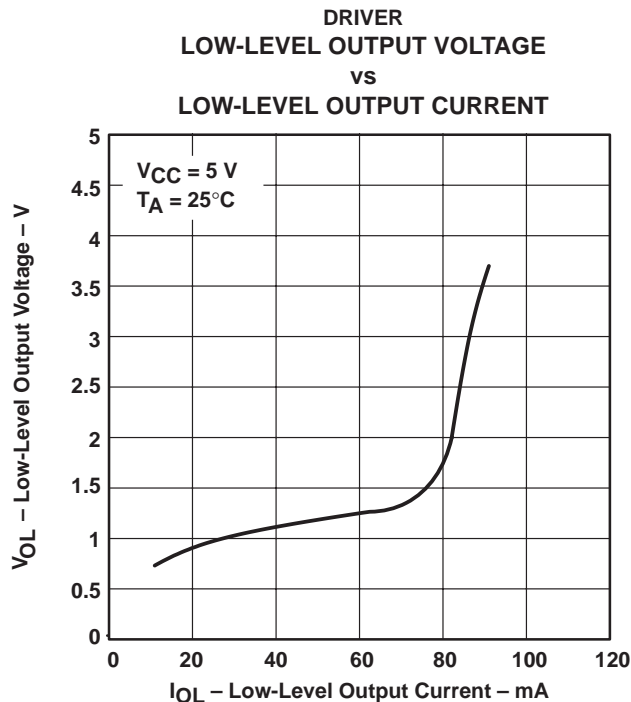
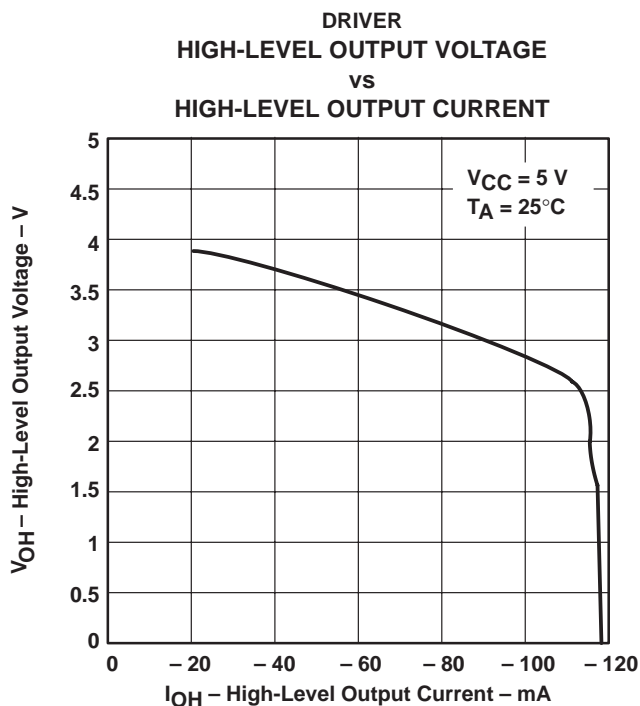
NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .

Figure 8. Receiver Test Circuit and Voltage Waveforms

# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040G – AUGUST 1987 – REVISED DECEMBER 1999

## TYPICAL CHARACTERISTICS†



† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

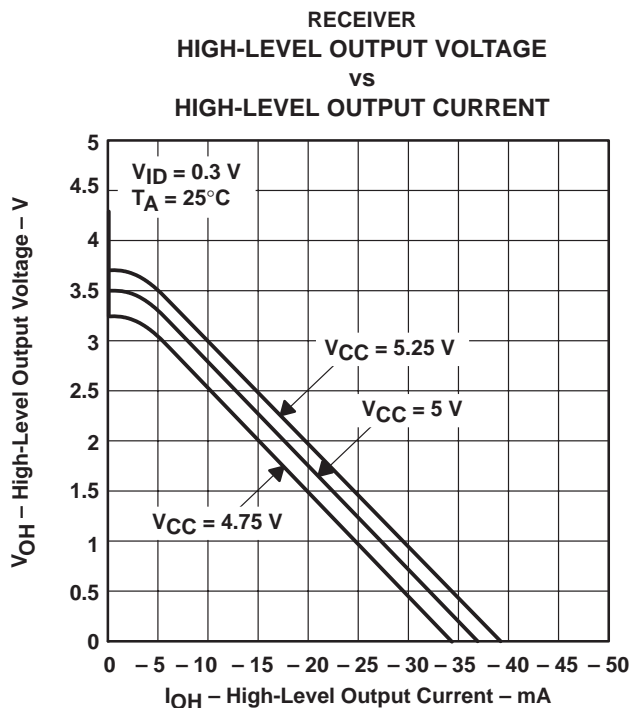


Figure 12

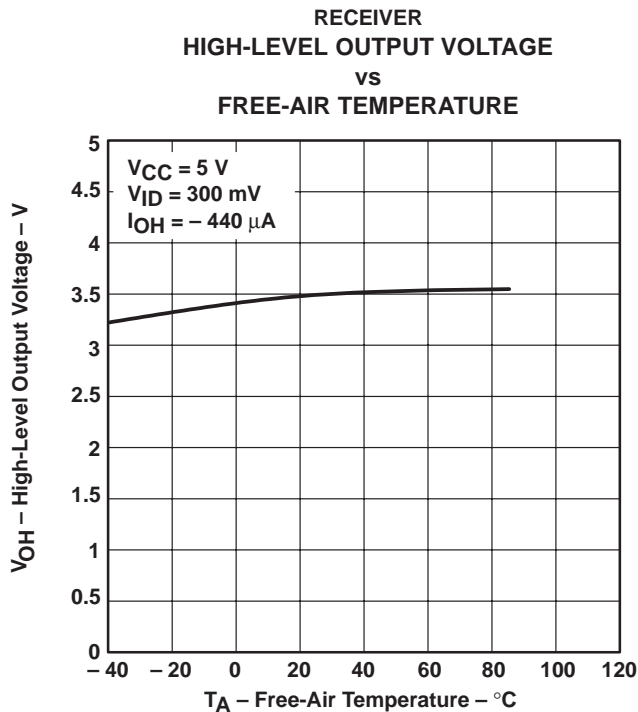


Figure 13

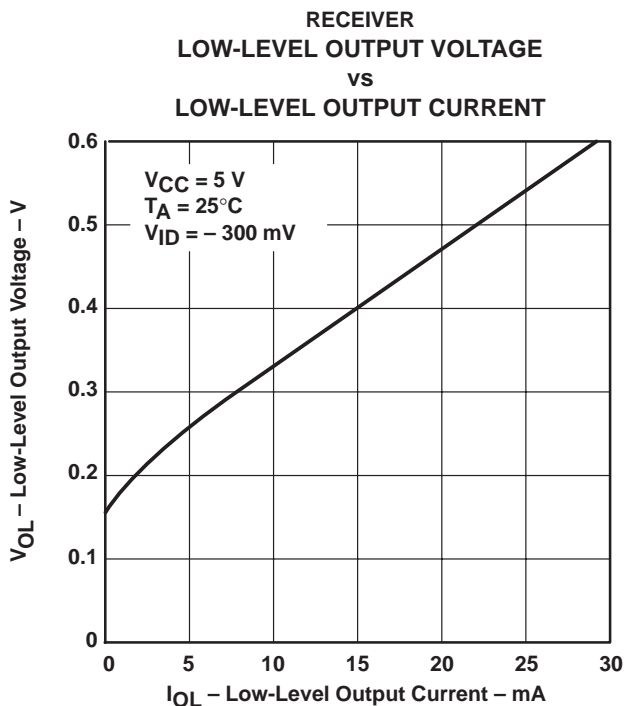


Figure 14

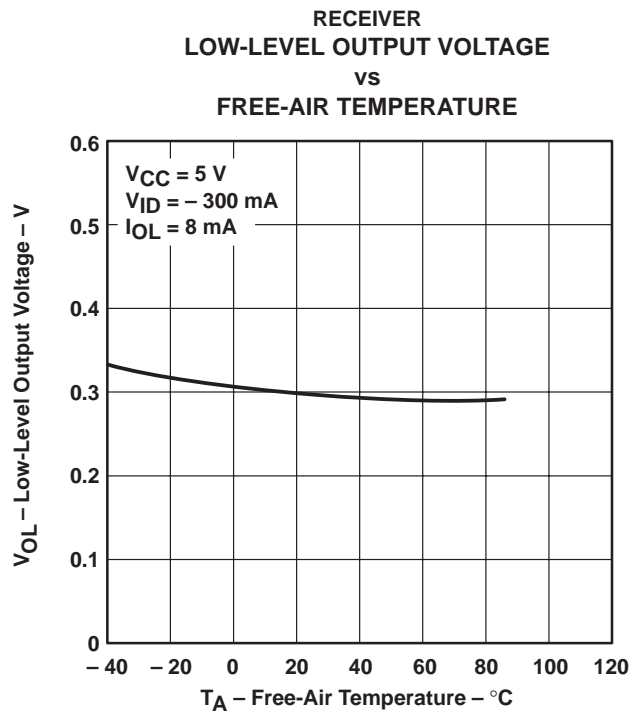


Figure 15

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

# SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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## TYPICAL CHARACTERISTICS†

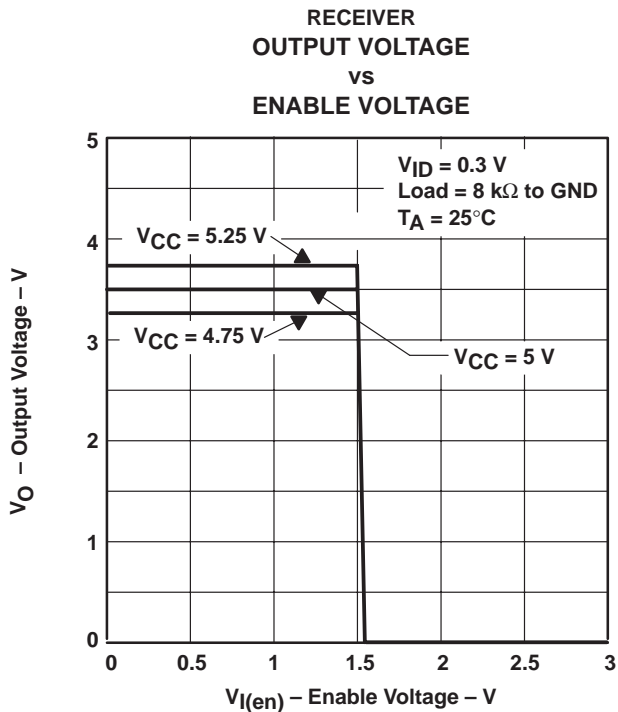


Figure 16

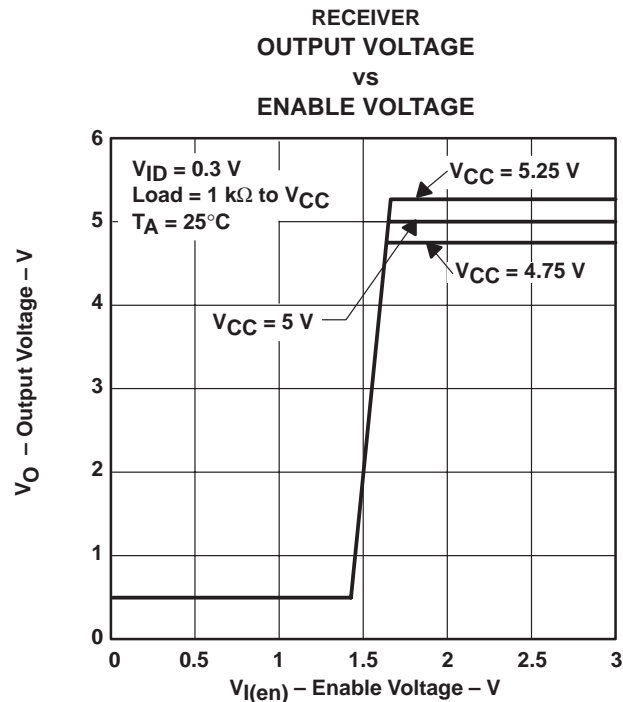
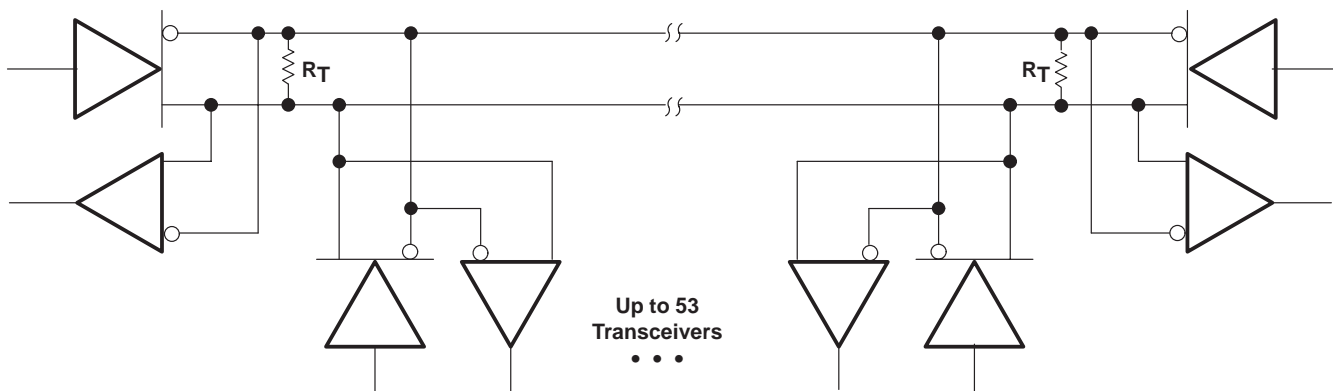


Figure 17

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

## APPLICATION INFORMATION



NOTE A: The line should terminate at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

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