



Micro Power Systems

MP1230/31/32

Microprocessor Compatible
Double-Buffered 12-Bit
Digital-to-Analog Converter

T-51-09-12

FEATURES

- Lower Data Bus Feedthrough @ $\overline{CS} = 1$
- Stable, More Accurate Segmented DAC Approach
- Ultra Stable
 - 0.2 ppm/°C Linearity Tempco
 - 2 ppm/°C Max. Gain Error Tempco
- Low Sensitivity to Amplifier V_{OS}
- $C_{OUT1} = 80$ pF at full scale, Gives Fastest Settling Times and Larger, Stable Bandwidth
- Lower Glitch Energy
- Four Quadrant Multiplication
- Low Feedthrough Error
- Low Power Consumption
- TTL/CMOS Compatible
- Latch-Up Free
- CDIP, PDIP and SOIC Packages Available

GENERAL DESCRIPTION

The MP1230/31/32 are 12-bit D/A Converters with 8/4 bit latched inputs for direct interface to the 8-bit data bus. All data loading and data transfer operations are identical to the WRITE cycle of a static RAM.

The MP1230 series uses a unique circuit which significantly reduces transients in the supplies during DATA bus transitions at $\overline{CS} = 1$.

The MP1230 series is manufactured using advanced thin film resistors on a double metal CMOS process. The MP1230 series incorporates a unique decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 12-bit linearity is achieved with minimal trimming. Outstanding features include:

- Stability: Both integral and differential linearity are rated at 0.2 ppm/°C typical, and monotonicity is guaranteed over the entire temperature range including the industrial and military ranges. Scale factor is a low 2 ppm/°C maximum.
- Low Output Capacitance: Due to smaller MOSFET switch geometries allowed by decoding, the output capacitance at

I_{OUT1} is a low 80pF / 40pF and 25pF / 65 pF at I_{OUT2} for the conditions of full scale/zero. This is over twice less than the National DAC1230 Series. Lower capacitance allows the MP1230 series to achieve faster CMOS DAC settling times; less than 1 μ sec for a 10 V step to 0.01% when utilizing a high speed output amplifier. Larger output amplifier bandwidths are available for a given amplifier loop gain because a smaller feedback "zero" compensating capacitor is required to offset the smaller I_{OUT} capacitance.

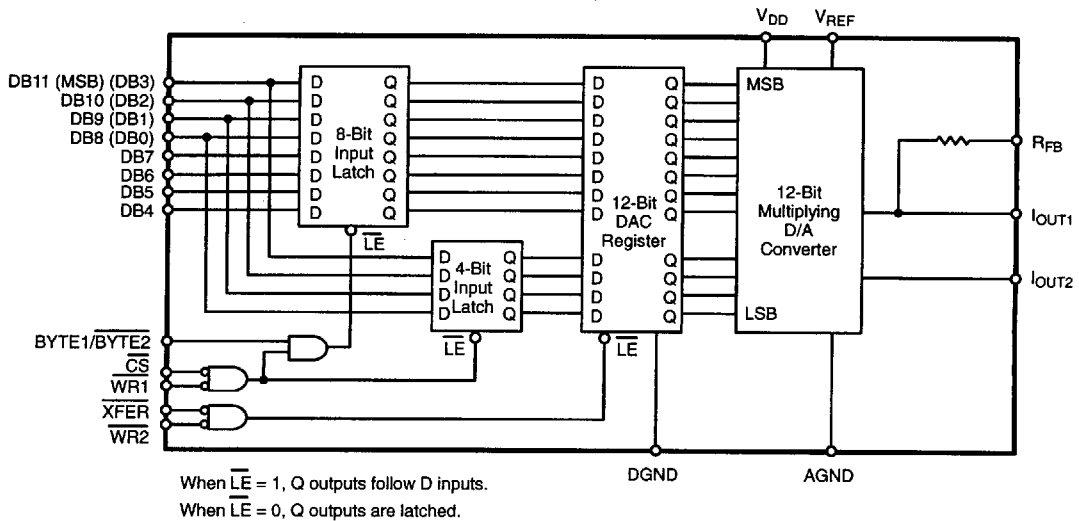
- Low Sensitivity to Output Amplifier Offset: 4 quadrant multiplying CMOS DACs provide an output current into the virtual ground of an op amp. The additional linearity error incurred by amplifier offset is reduced by a factor of 2 in the MP1208/1230 series over conventional R-2R DACs, to 330 μ V per millivolt of offset.

Specified for operation over the commercial / industrial (–40 to +85°C) and military (–55 to +125°C) temperature ranges, the MP1230/31/32 are available in Plastic (PDIP) and Ceramic (CDIP) dual-in-line, and Small Outline (SOIC) packages.

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SIMPLIFIED BLOCK DIAGRAM



ORDERING INFORMATION

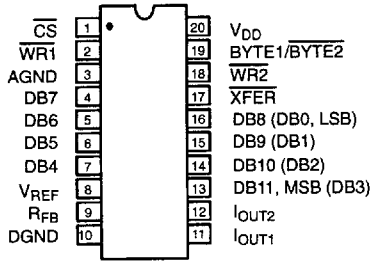
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	-40 to +85°C	MP1231JN	±1	±1	±0.4
Plastic Dip	-40 to +85°C	MP1230KN	±1/2	±3/4	±0.4
Plastic Dip	-40 to +85°C	MP1232HN	±2	±2	±0.4
SOIC	-40 to +85°C	MP1231JS	±1	±1	±0.4
Ceramic Dip	-40 to +85°C	MP1231AD	±1	±1	±0.4
Ceramic Dip	-40 to +85°C	MP1230BD	±1/2	±3/4	±0.4
Ceramic Dip	-40 to +85°C	MP1232ZD	±2	±2	±0.4
Ceramic Dip	-55 to +125°C	MP1231SD	±1	±1	±0.4
Ceramic Dip	-55 to +125°C	MP1231SD/883	±1	±1	±0.4
Ceramic Dip	-55 to +125°C	MP1230TD	±1/2	±3/4	±0.4
Ceramic Dip	-55 to +125°C	MP1230TD/883	±1/2	±3/4	±0.4
Ceramic Dip	-55 to +125°C	MP1232RD	±2	±2	±0.4
Ceramic Dip	-55 to +125°C	MP1232RD/883	±2	±2	±0.4



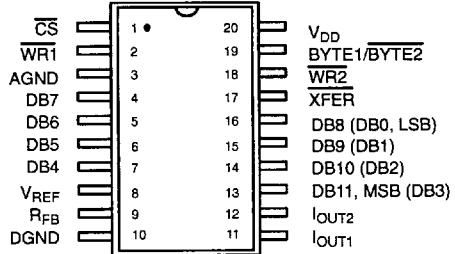
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PIN CONFIGURATIONS



20 Pin CDIP, PDIP (0.300")
D20, N20



20 Pin SOIC (Jedec, 0.300")
S20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	CS	Chip Select (Active Low)
2	WR1	Write 1 (Active Low)
3	AGND	Analog Ground
4	DB7	Data Input Bit 7
5	DB6	Data Input Bit 6
6	DB5	Data Input Bit 5
7	DB4	Data Input Bit 4
8	V _{REF}	Reference Input Voltage
9	R _{FB}	Internal Feedback Resistor
10	DGND	Digital Ground
11	I _{OUT1}	Current Output 1
12	I _{OUT2}	Current Output 2
13	DB11 (DB3)	Data Input Bit 9 (MSB)
14	DB10 (DB2)	Current Output 10
15	DB9 (DB1)	Data Input Bit 9
16	DB8 (DB0)	Data Input Bit 8 (LSB)
17	XFER	Transfer Control Signal (Active Low)
18	WR2	Write 2 (Active Low)
19	BYTE1/ BYTE2	Byte Sequence Control
20	V _{DD}	Positive Power Supply



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ELECTRICAL CHARACTERISTICS

($V_{DD} = +15\text{ V}$, $V_{REF} = +10\text{ V}$ unless otherwise noted)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
STATIC PERFORMANCE (1)								
Resolution (All Grades)	N	12			12			FSR = Full Scale Range Bits
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL - Min INL) / 2
MP1230				±1/2		±1/2		
MP1231				±1		±1		
MP1232				±2		±2		
Differential Non-Linearity	DNL						LSB	
MP1230				±3/4		±3/4		
MP1231				±1		±1		
MP1232				±2		±2		
Gain Error	GE	±0.1	±0.4			±0.4	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient (2)	TC_{GE}	1				±2	ppm/°C	$\Delta\text{Gain}/\Delta\text{Temperature}$
Power Supply Rejection Ratio	PSRR	5	±20			±20	ppm/%	$ \Delta\text{Gain}/\Delta V_{DD} \Delta V_{DD} = \pm 5\%$
Output Leakage Current	I_{OUT}	1	±10			±200	nA	
DYNAMIC PERFORMANCE (2)								
Current Settling Time	t_S	1.0					μsec	$R_L=100\Omega$, $C_L=13\text{pF}$
AC Feedthrough at I_{OUT1}	F_T	1.0					mV p-p	Full Scale Change to 1/2 LSB $V_{REF}=100\text{kHz}$, 20Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS (3)								
Logical "1" Voltage	V_{IH}	2.4			2.4		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}	0.1	±1			±1	μA	
ANALOG OUTPUTS (2)								
Output Capacitance	C_{OUT1}	80	100				pF	DAC Inputs all 1's
	C_{OUT1}	40	60				pF	DAC Inputs all 0's
	C_{OUT2}	65	85				pF	DAC Inputs all 1's
	C_{OUT2}	25	45				pF	DAC Inputs all 0's
POWER SUPPLY								
Functional Voltage Range (5)	V_{DD}	4.5	15	16			V	
Supply Current	I_{DD}	1.2	2			2	mA	All digital inputs = 0 V or all = 5 V



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ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
SWITCHING CHARACTERISTICS (2, 4)								
WR, XFER Pulse Width	t _{WR}	100	50				ns	
Data Set-Up Time	t _{DS}	100	50				ns	
Data Hold Time	t _{DH}	90	70				ns	
CS Set-Up Time	t _{CS}	200	100				ns	
CS Hold Time	t _{CH}	10	0				ns	

NOTES:

- (1) Full Scale Range (FSR) is 10V.
- (2) Guaranteed but not production tested
- (3) Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- (4) See switching waveforms
- (5) Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

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ABSOLUTE MAXIMUM RATINGS (1, 2, 3) (TA = +25°C unless otherwise noted)

V _{DD} to GND +17 V	Storage Temperature -65°C to +150°C
Digital Input Voltage to GND GND -0.5 to V _{DD} +0.5 V	Lead Temperature (Soldering, 10 seconds) +300°C
I _{OUT1} , I _{OUT2} to GND GND -0.5 to V _{DD} +0.5 V	Package Power Dissipation Rating to 75°C	
V _{REF} to GND ±25 V	CDIP, PDIP, SOIC 900mW
V _{RFB} to GND ±25 V	Derates above 75°C 12mW/°C
AGND to DGND ±1 V		
(Functionality Guaranteed ±0.5 V)			

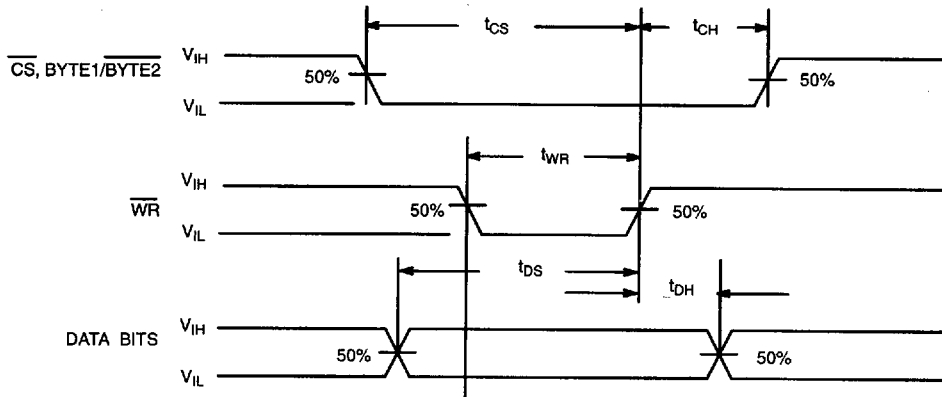
NOTES:

- (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- (2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
- (3) GND refers to AGND and DGND.

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SWITCHING WAVEFORMS



DEFINITION OF CONTROL SIGNALS:

\overline{CS} : Chip Select. (Active low)
It will enable WR1.

$\overline{WR1}$: Write 1 (Active low)
The $\overline{WR1}$ is used to load the digital data bits (DB) into the input latch.

$\overline{BYTE 1/BYTE 2}$: Byte sequence control.
The $\overline{BYTE 1/BYTE 2}$ control pin is used to select both MSB and LSB input latches.

$\overline{WR2}$: Write 2 (Active low)
It will enable \overline{XFER} .

\overline{XFER} : Transfer control signal (Active low)
This signal in combination with $\overline{WR2}$ causes the 16-bit data which is available in the input latches to transfer to the DAC register.

DB0 to DB11: Digital Inputs.
DB0 is the least significant digital input (LSB) and DB11 is the most significant digital input (MSB).

I_{OUT1} : DAC Current Output 1 Bus.
 I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in the DAC register.

I_{OUT2} : DAC Current Output 2 Bus.
 I_{OUT2} is a complement of I_{OUT1} .

R_{FB} : Feedback Resistor.
This internal feedback resistor should always be used (not an external resistor) since it matches the resistors in the DAC and tracks these resistors over temperature.

V_{REF} : Reference Voltage Input.
This input connects an external precision voltage source to the internal DAC. The V_{REF} can be selected over the range of +25V to -25V or the analog signal for a 4-quadrant multiplying mode application.

V_{DD} : Power Supply Voltage.
This is the power supply pin for the part. The V_{DD} can be from +5 V DC to +15 V DC, however optimum voltage is +12 to +15 V DC.

AGND: Analog Ground
Back gate of the DAC N-channel current steering switches.

DGND: Digital Ground



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APPLICATION NOTES

Refer to Section 8 for Applications Information

The MP1230 series allows direct interface to microprocessor system buses without the need for additional interface circuitry. They provide 8 data input lines in parallel for optimum interface to a 16-bit data bus, but can be mapped onto an 8-bit bus by tying lines DB0 through DB3 to lines DB8 through DB11, respectively.

All digital inputs maintain TTL compatibility over the entire range of V_{DD} . The internal latches are level-triggered, and therefore can be hardwired for transparent operation. The MP1208 series can be wired for a single layer of buffering by tying the 12 bit DAC register transparent (ground \overline{XFER} and $\overline{WR2}$) or by tying the 8-bit and 4-bit latch transparent (ground \overline{CS} , $\overline{WR1}$, $\overline{BYTE1/BYTE2} = V_{DD}$). In non-microprocessor applications, the MP1230 series can be wired for flow-through operation. The analog output will continuously reflect the state of the digital inputs by tying the 8-bit latch, 4-bit latch, and 12-bit DAC register transparent.

Double-buffering provides the user with the capability of refreshing simultaneously all 12 data bits to the DAC from an 8-bit

data bus. Double-buffering also allows a single DAC or several DACs to be updated from the same data bus at the same time. This will be done asynchronously by an external monitoring device (such as a voltage comparator) or by a system interrupt. In this example, tie $\overline{WR2}$ low and use the \overline{XFER} to update the 12-bit register.

For a two byte load, tie $\overline{BYTE1/BYTE2}$ and \overline{XFER} together and $\overline{WR1}$ and $\overline{WR2}$ together. The first write will update the 8-bit input latch (the 4-bit latch is also changed). The second write will overwrite the 4-bit latch and transfer all 12 bits to the 12-bit DAC register, updating the DAC. (See *Typical Application*.)

Use the high order address lines for the device select (\overline{CS}). Normally the low order address lines ($A0, A1$) will be decoded for $\overline{BYTE1/BYTE2}$ and \overline{XFER} . The \overline{XFER} input can be decoded independently (3 write loads) when independent control is desired.

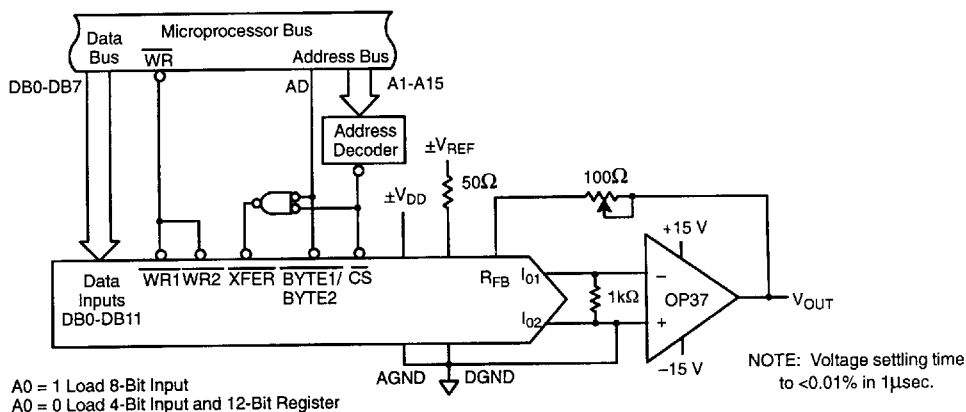


Figure 1. Two Write Load / Unipolar Configuration