19-0378; Rev 1; 6/95

MAXIM

# Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs



## General Description

The MAX521 is an octal, 8-bit voltage-output digital-to-analog converter (DAC) with a simple 2-wire serial interface that allows communication between multiple devices. It operates from a single 5V supply and its internal precision buffers allow the DAC outputs to swing rail-to-rail. The reference input range includes both supply rails.

The MAX521 has five reference inputs. The first four DACs (DAC0–DAC3) each have a separate reference input (REF0–REF3), allowing each DAC's full-scale range to be set independently. The remaining four DACs (DAC4–DAC7) share the remaining reference input, REF4.

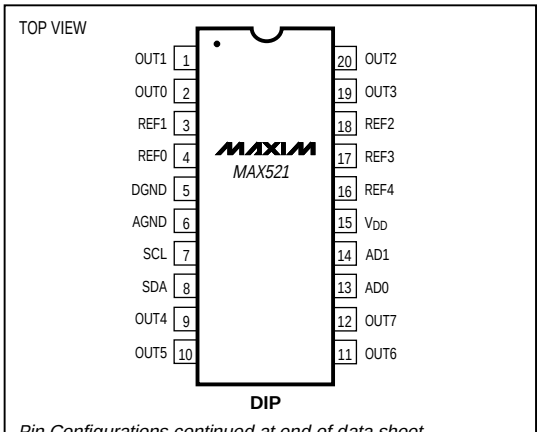
The MAX521 features a serial interface and internal software protocol, allowing communication at data rates up to 400kbps. The interface, combined with the double-buffered input configuration, allows the DAC registers to be updated individually or simultaneously. In addition, the device can be put into a low-power shutdown mode that reduces supply current to 4µA. Power-on reset ensures the DAC outputs are at 0V when power is initially applied.

The MAX521 is available in 20-pin DIP and 24-pin SO package as well as a space-saving 24-pin SSOP package.

## Applications

Minimum Component Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Automatic Test Equipment
Programmable Attenuators

## Pin Configurations




*Pin Configurations continued at end of data sheet.*

## Features

- **Single +5V Supply**
- **Simple 2-Wire Serial Interface**
- **I²C Compatible**
- **Output Buffer Amplifiers Swing Rail-to-Rail**
- **Reference Input Range Includes Both Supply Rails**
- **Power-On Reset Clears All Latches**
- **4µA Power-Down Mode**

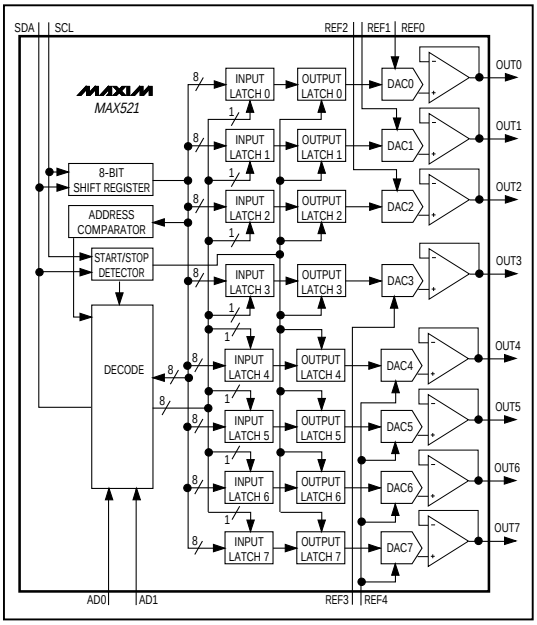
## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE | TUE (LSB) |
|---|---|---|---|
| MAX521ACPP | 0°C to +70°C | 20 Plastic DIP | 1 |
| MAX521BCPP | 0°C to +70°C | 20 Plastic DIP | 2 |
| MAX521ACWG | 0°C to +70°C | 24 Wide SO | 1 |
| MAX521BCWG | 0°C to +70°C | 24 Wide SO | 2 |
| MAX521ACAG | 0°C to +70°C | 24 SSOP | 1 |
| MAX521BCAG | 0°C to +70°C | 24 SSOP | 2 |
| MAX521BC/D | 0°C to +70°C | Dice* | 2 |

***Ordering Information continued at end of data sheet.***

**Dice are specified at $T_A$ = +25°C, DC parameters only.*

## Functional Diagram



# Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to DGND .....-0.3V to +6V
$V_{DD}$ to AGND.....-0.3V to +6V
OUT0–OUT7.....-0.3V to ($V_{DD}$ + 0.3V)
REF0–REF4.....-0.3V to ($V_{DD}$ + 0.3V)
AD0, AD1.....-0.3V to ($V_{DD}$ + 0.3V)
SCL, SDA to DGND.....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation ($T_A$ = +70°C)
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C)....889mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C) ....941mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) .....640mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C)....889mW
Operating Temperature Ranges
MAX521_C_ _ .....0°C to +70°C
MAX521_E_ _.....-40°C to +85°C
MAX521BMJP.....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 5V ±10%, $V_{REF\_}$ = 4V, $R_L$ = 10kΩ, $C_L$ = 100pF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **STATIC ACCURACY** | | | | | | | |
| Resolution | | | | 8 | | | Bits |
| Total Unadjusted Error | TUE | | MAX521A | | | ±1.5 | LSB |
| | | | MAX521B | | | ±2.0 | |
| Differential Nonlinearity | DNL | Guaranteed monotonic | | | | ±1.0 | LSB |
| Zero-Code-Error | ZCE | Code = 00 hex | MAX521_C | | | 18 | mV |
| | | | MAX521_E | | | 20 | |
| | | | MAX521BM | | | 20 | |
| Zero-Code-Error Supply Rejection | | Code = 00 hex | MAX521_C | | ±1 | | mV |
| | | | MAX521_E | | ±1 | | |
| | | | MAX521BM | | ±1 | | |
| Zero-Code-Error Temperature Coefficient | | Code = 00 hex | | | ±10 | | µV/°C |
| Full-Scale Error | | Code = FF hex | MAX521_C | | | 18 | mV |
| | | | MAX521_E | | | 20 | |
| | | | MAX521BM | | | 20 | |
| Full-Scale-Error Supply Rejection | | Code = FF hex $V_{DD}$ = 5V ±10% | MAX521_C | | ±1 | | mV |
| | | | MAX521_E | | ±1 | | |
| | | | MAX521BM | | ±1 | | |
| Full-Scale-Error Temperature Coefficient | | | | | ±10 | | µV/°C |
| **REFERENCE INPUTS** | | | | | | | |
| Input Voltage Range | | | | 0 | | $V_{DD}$ | V |
| Input Resistance | $R_{IN}$ | Code = 55 hex (Note 1) | REF4 | 4 | 6 | | kΩ |
| | | | REF0–REF3 | 16 | 24 | | |
| Input Current | | PD = 1 | | | | ±10 | µA |
| Input Capacitance | | Code = FF hex (Note 2) | REF4 | | 120 | | pF |
| | | | REF0–REF3 | | 30 | | |
| Channel-to-Channel Isolation | | (Note 3) | | | -60 | | dB |
| AC Feedthrough | | (Note 4) | | | -70 | | dB |

**Note 1:** Input resistance is code dependent. The lowest input resistance occurs at code = 55 hex.
**Note 2:** Input capacitance is code dependent. The highest input capacitance occurs at code = FF hex.
**Note 3:** $V_{REF}$ = 4Vp-p, 10kHz. Channel-to-channel isolation is measured by setting the code of one DAC to FF hex and setting the code of all other DACs to 00 hex.
**Note 4:** $V_{REF}$ = 4Vp-p, 10kHz, DAC code = 00 hex.

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 5V ±10%, $V_{REF\_}$ = 4V, $R_L$ = 10kΩ, $C_L$ = 100pF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DAC OUTPUTS** | | | | | | | |
| Full-Scale Output Voltage | | | | 0 | | $V_{DD}$ | V |
| Output Load Regulation | | OUT_ = 4V, 0mA to 2.5mA | | | 0.25 | | LSB |
| | | $V_{REF\_}$ = $V_{DD}$, code = FF hex, 0µA to 500µA, MAX521_C/E | | | 1.5 | | |
| | | $V_{REF\_}$ = $V_{DD}$, code = FF hex, 0µA to 500µA, MAX521BM | | | 2.0 | | |
| Output Leakage Current | | OUT_ = 0V to $V_{DD}$, PD = 1 | | | | ±10 | µA |
| **DIGITAL INPUTS SCL, SDA** | | | | | | | |
| Input High Voltage | $V_{IH}$ | | | 0.7$V_{DD}$ | | | V |
| | $V_{IL}$ | | | | | 0.3$V_{DD}$ | |
| Input Current | $I_{IN}$ | 0V ≤ $V_{IN}$ ≤ $V_{DD}$ | | | | ±10 | µA |
| Input Hysteresis | $V_{HYST}$ | (Note 5) | | 0.05$V_{DD}$ | | | V |
| Input Capacitance | $C_{IN}$ | (Note 5) | | | | 10 | pF |
| **DIGITAL INPUTS AD0, AD1** | | | | | | | |
| Input High Voltage | $V_{IN}$ | | | 2.4 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | | 0.8 | V |
| Input Leakage | $I_{IN}$ | $V_{IN}$ = 0V to $V_{DD}$ | | | | ±10 | µA |
| **DIGITAL OUTPUT SDA** (Note 6) | | | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 3mA | | | | 0.4 | V |
| | | $I_{SINK}$ = 6mA | | | | 0.6 | |
| Three-State Leakage Current | $I_L$ | $V_{IN}$ = 0V to $V_{DD}$ | | | | ±10 | µA |
| Three-State Output Capacitance | $C_{OUT}$ | (Note 5) | | | | 10 | pF |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Voltage Output Slew Rate | | Positive and negative | MAX521_C | | 1.0 | | V/µs |
| | | | MAX521_E | | 0.7 | | |
| | | | MAX521BM | | 0.5 | | |
| Output Settling Time | | To 1/2 LSB, 10kΩ and 100pF load (Note 7) | | | 6 | | µs |
| Digital Feedthrough | | Code = 00 hex, all digital inputs from 0V to $V_{DD}$ | | | 5 | | nV-s |
| Digital-Analog Glitch Impulse | | Code 128 to 127 | | | 12 | | nV-s |
| Signal to Noise + Distortion Ratio | SINAD | $V_{REF\_}$ = 4Vp-p at 1kHz, $V_{DD}$ = 5V, Code = FF hex | | | 87 | | dB |
| Multiplying Bandwidth | | $V_{REF\_}$ = 4Vp-p, 3dB bandwidth | | | 1 | | MHz |
| Wideband Amplifier Noise | | | | | 60 | | $µV_{RMS}$ |
| **POWER REQUIREMENTS** | | | | | | | |
| Supply Voltage | $V_{DD}$ | | | 4.5 | | 5.5 | V |
| Supply Current | $I_{DD}$ | Normal mode, output unloaded, all digital inputs 0V or $V_{DD}$ | MAX521_C | | 10 | 20 | mA |
| | | | MAX521_E/BM | | 10 | 24 | |
| | | Power-down mode (PD = 1) | | | 4 | 20 | µA |

**Note 5:** Guaranteed by design.
**Note 6:** $I^2C$ compatible mode.
**Note 7:** Output settling time is measured by taking the code from 00 hex to FF hex, and from FF hex to 00 hex.

## TIMING CHARACTERISTICS

($V_{DD}$ = 5V ±10%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are $T_A$ = +25°C.)

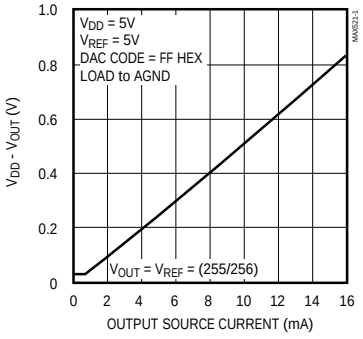
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Serial Clock Frequency | $f_{SCL}$ | | 0 | | 400 | kHz |
| Bus Free Time Between a STOP and a START Condition | $t_{BUF}$ | | 1.3 | | | µs |
| Hold Time, (Repeated) Start Condition | $t_{HD, STA}$ | | 0.6 | | | µs |
| LOW Period of the SCL Clock | $t_{LOW}$ | | 1.3 | | | µs |
| High Period of the SCL Clock | $t_{HIGH}$ | | 0.6 | | | µs |
| Setup Time for a Repeated START Condition | $t_{SU, STA}$ | | 0.6 | | | µs |
| Data Hold Time | $t_{HD, DAT}$ | (Note 8) | 0 | | 0.9 | µs |
| Data Setup Time | $t_{SU, DAT}$ | | 100 | | | ns |
| Rise Time of Both SDA and SCL Signals, Receiving | $t_R$ | (Note 9) | 20 + 0.1Cb | | 300 | ns |
| Fall Time of Both SDA and SCL Signals, Receiving | $t_F$ | (Note 9) | 20 + 0.1Cb | | 300 | ns |
| Fall Time of SDA Transmitting (Note 6) | $t_F$ | $I_{SINK} \le$ 6mA (Note 9) | 20 + 0.1Cb | | 250 | ns |
| Setup Time for STOP Condition | $t_{SU, STO}$ | | 0.6 | | | µs |
| Capacitive Load for Each Bus Line | Cb | | | | 400 | pF |
| Pulse Width of Spike Suppressed | $t_{SP}$ | (Notes 10, 11) | 0 | | 50 | ns |

**Note 8:** A master device must provide a hold time of at least 300ns for the SDA signal (referred to $V_{IL}$ of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
**Note 9:** Cb = total capacitance of one bus line in pF. $t_R$ and $t_f$ measured between 0.3$V_{DD}$ and 0.7$V_{DD}$.
**Note 10:** An input filter on the SDA and SCL input suppresses noise spikes less than 50ns.
**Note 11:** Guaranteed by design.

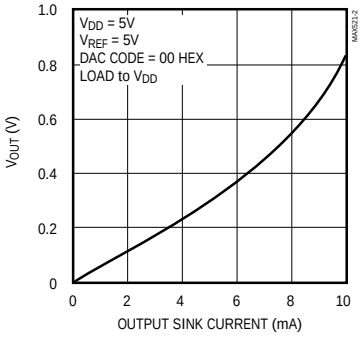
## Typical Operating Characteristics

($T_A$ = +25°C, unless otherwise noted.)

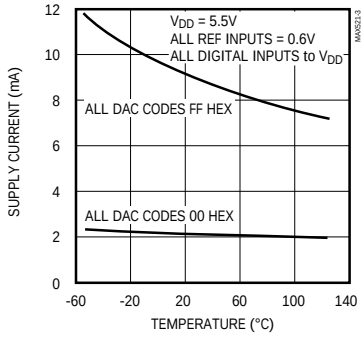
**DAC OUTPUT HIGH VOLTAGE vs. OUTPUT SOURCE CURRENT**




**DAC OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT**



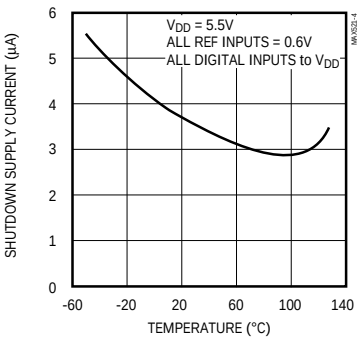

**SUPPLY CURRENT vs. TEMPERATURE**



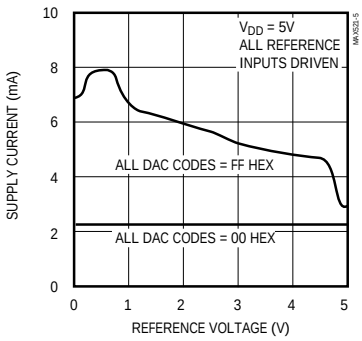
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

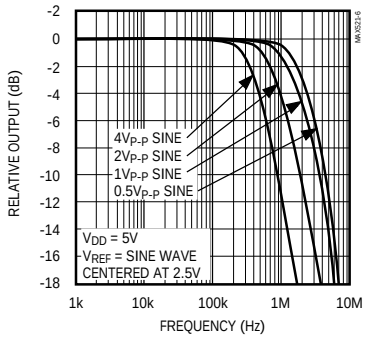
**SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE**



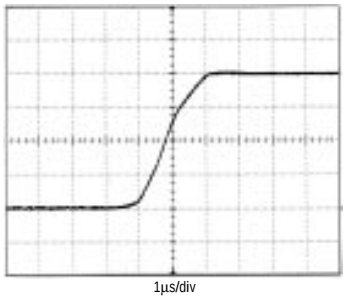

**SUPPLY CURRENT vs. REFERENCE VOLTAGE**




**REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE**

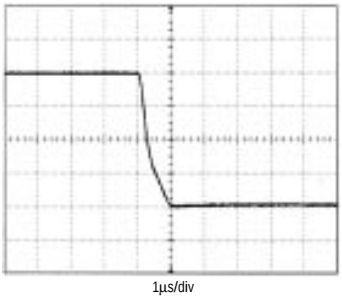



**POSITIVE SETTLING TIME**



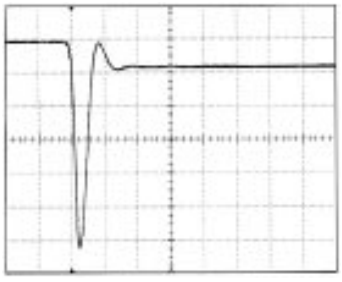

OUT1 LOADED WITH 10kΩ II 100pF
REF1 = 4V
DAC CODE = 00 HEX to FF HEX

**NEGATIVE SETTLING TIME**




OUT1 LOADED WITH 10kΩ II 100pF
REF1 = 4V
DAC CODE = FF HEX to 00 HEX

**WORST-CASE 1LSB DIGITAL STEP CHANGE**



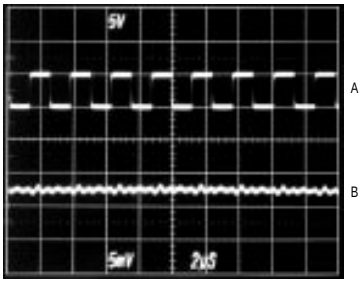

REF1 = 5V
DAC CODE = 80 HEX to 7F HEX

# Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

## Typical Operating Characteristics (continued)

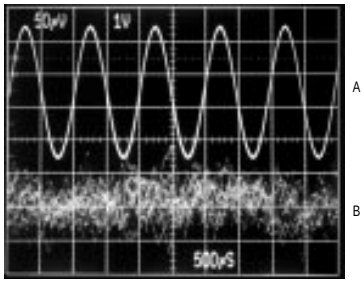
($T_A$ = +25°C, unless otherwise noted.)

**CLOCK FEEDTHROUGH**



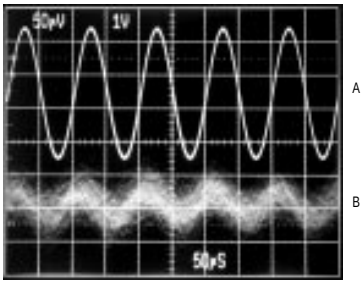

A = SCL, 400kHz, 5V/div
B = OUT1, 5mV/div
DAC CODE = 7F HEX
REF1 = 5V

**REFERENCE FEEDTHROUGH AT 1kHz**



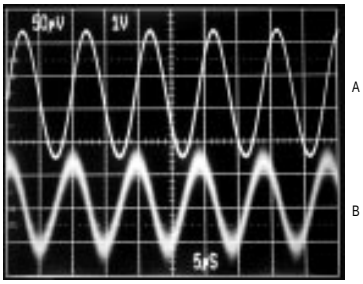

A = REF1, 1V/div ($4V_{P-P}$)
B = OUT1, 50µV/div, UNLOADED
FILTER PASSBAND = 100Hz to 10kHz
DAC CODE = 00 HEX

**REFERENCE FEEDTHROUGH AT 10kHz**




A = REF1, 1V/div ($4V_{P-P}$)
B = OUT1, 50µV/div, UNLOADED
FILTER PASSBAND = 1kHz to 100kHz
DAC CODE = 00 HEX

**REFERENCE FEEDTHROUGH AT 100kHz**




A = REF1, 1V/div ($4V_{P-P}$)
B = OUT1, 50µV/div, UNLOADED
FILTER PASSBAND = 10kHz to 1MHz
DAC CODE = 00 HEX

## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| DIP | SO/SSOP | | |
| 1 | 1 | OUT1 | DAC1 Voltage Output |
| 2 | 2 | OUT0 | DAC0 Voltage Output |
| 3 | 3 | REF1 | Reference Voltage Input for DAC1 |
| 4 | 4 | REF0 | Reference Voltage Input for DAC0 |
| — | 7, 9, 16, 20 | N.C. | No Connect—not internally connected. |
| 5 | 5 | DGND | Digital Ground |
| 6 | 6 | AGND | Analog Ground |
| 7 | 8 | SCL | Serial Clock Input |
| 8 | 10 | SDA | Serial Data Input |
| 9 | 11 | OUT4 | DAC4 Voltage Output |
| 10 | 12 | OUT5 | DAC5 Voltage Output |
| 11 | 13 | OUT6 | DAC6 Voltage Output |
| 12 | 14 | OUT7 | DAC7 Voltage Output |
| 13 | 15 | AD0 | Address Input 0; sets IC's slave address |
| 14 | 17 | AD1 | Address Input 1; sets IC's slave address |
| 15 | 18 | $V_{DD}$ | Power Supply, +5V |
| 16 | 19 | REF4 | Reference Voltage Input for DACs 4, 5, 6, and 7 |
| 17 | 21 | REF3 | Reference Voltage Input for DAC3 |
| 18 | 22 | REF2 | Reference Voltage Input for DAC2 |
| 19 | 23 | OUT3 | DAC3 Voltage Output |
| 20 | 24 | OUT2 | DAC2 Voltage Output |

## Detailed Description

### Serial Interface

The MAX521 uses a simple two-wire serial interface requiring only two I/O lines (2-wire bus) of a standard microprocessor port. Figure 1 shows the timing diagram for signals on the wire bus. Figure 2 shows the typical application of the MAX521. The 2-wire bus can have several devices (in addition to the MAX521) attached. The two bus lines (SDA and SCL) must be high when the bus is not in use. When in use, the port bits are toggled to generate the appropriate signals for SDA and SCL. External pull-up resistors are not required on these lines. The MAX521 can be used in applications where pull-up resistors are required (such as in $I^2C$ systems) to maintain compatibility with the existing circuitry.

The MAX521 is a receive-only device and must be controlled by a bus master device. The MAX521 operates at SCL rates up to 400kHz. A master device sends information to the MAX521 by transmitting the MAX521's address over the bus and then transmitting the desired information. Each transmission consists of a START condition, the MAX521's programmable slave-address, one or more command-byte/output-byte pairs (or a command byte alone, if it is the last byte in the transmission), and finally, a STOP condition (Figure 3).

The address byte and pairs of command and output bytes are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low. The only exceptions to this are the START and STOP conditions. SDA's state is sampled, and therefore must remain stable while SCL is high. Data is transmitted in 8-bit bytes. Nine clock cycles are required to transfer the data bits to the MAX521. Set SDA low during the 9th clock cycle as the MAX521 pulls SDA low during this time. $R_C$ (see Figure 2) limits the current that flows during this time if SDA stays high for short periods of time.

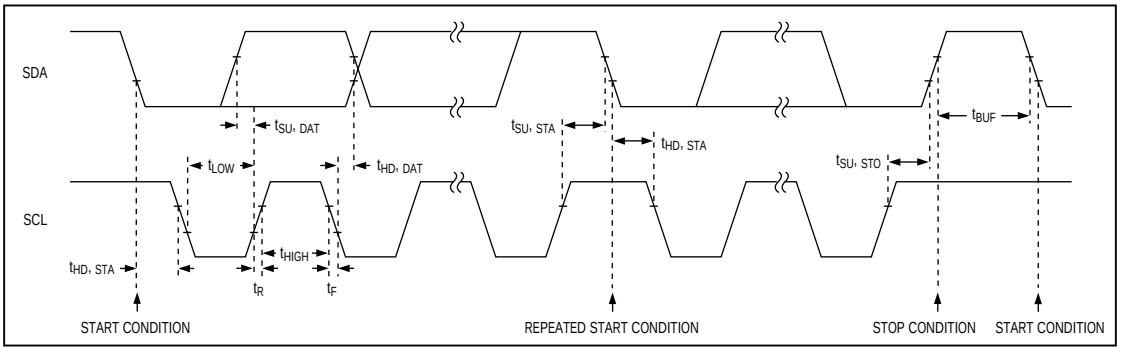



*Figure 1. Two-Wire Serial Interface Timing Diagram*

# Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

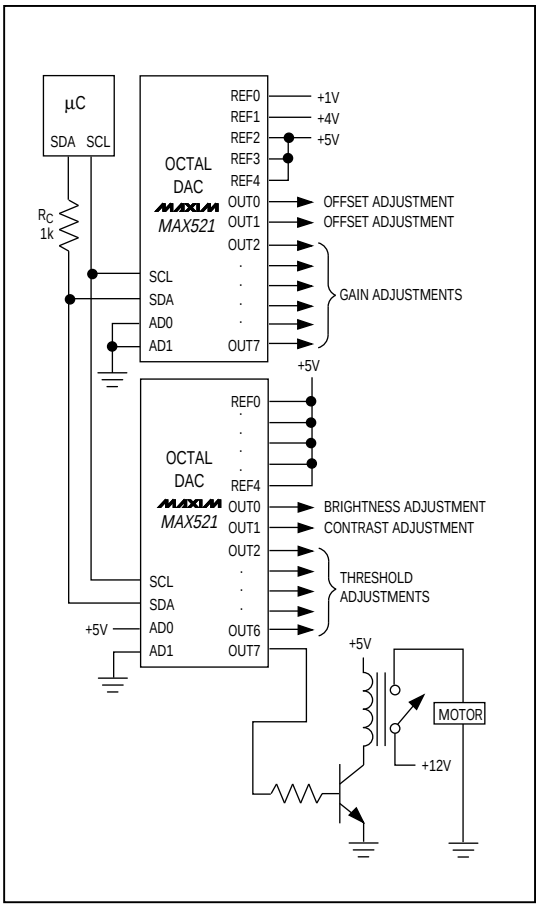



*Figure 2. MAX521 Typical Application Circuit*

### *The START and STOP Conditions*

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 4). When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

### *The Slave Address*

The MAX521's slave address is seven bits long (Figure 5). The first five bits (MSBs) of the slave address have been factory programmed and are always 01010. The state of the MAX521 inputs AD0 and AD1 determine the final two bits of the 7-bit slave address. These input pins may be connected to $V_{DD}$ or DGND, or they may be actively driven by TTL or CMOS logic levels. There are four possible slave addresses for the MAX521, and therefore a maximum of four such devices may be on the bus at one time. The eighth bit (LSB) in the slave address byte should be low when writing to the MAX521.

The MAX521 watches the bus continuously, waiting for a START condition followed by its slave address. When it recognizes its slave address, it is ready to accept data.

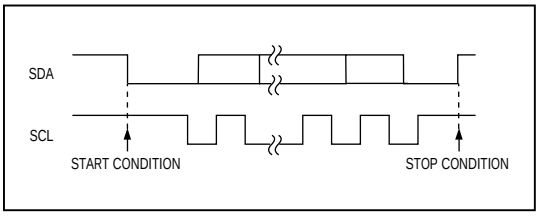



*Figure 4. All communications begin with a START condition and end with a STOP condition, both generated by a bus master.*

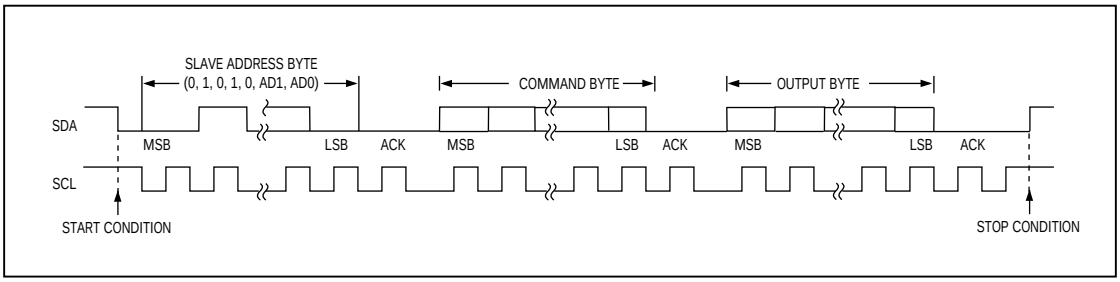



*Figure 3. A Complete Serial Transmission*

***The Command Byte and Output Byte***

A command byte follows the slave address. Figure 6 shows the format for the command byte. A command byte is usually followed by an output byte unless it is the last byte in the transmission. If it is the last byte, all bits except PD and RST are ignored. If an output byte follows the command byte, A0–A2 of the command byte indicate the digital address of the DAC whose input data latch receives the digital output data. The data is transferred to the DAC's output latch during the STOP condition following the transmission. This allows all DACs to be updated and the new outputs to appear simultaneously (Figure 7).

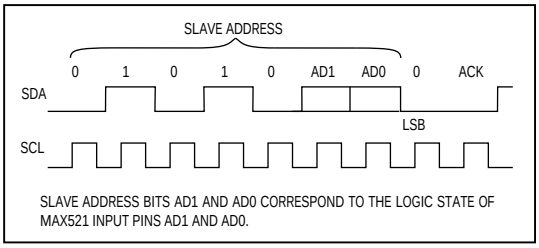
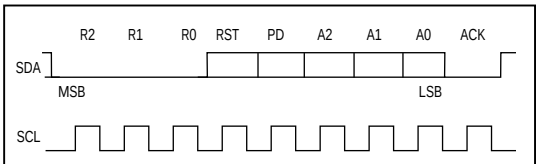



*Figure 5. Address Byte*




| | |
|---|---|
| R2, R1, R0: | RESERVED BITS. SET TO 0. |
| RST: | RESET BIT, SET TO 1 TO RESET ALL DAC REGISTERS. |
| PD: | POWER-DOWN BIT. SET TO 1 TO PLACE THE MAX521 IN THE 10µA SHUTDOWN MODE. SET TO 0 TO RETURN THE MAX521 TO THE NORMAL OPERATIONAL STATE. |
| A2, A1, A0: | ADDRESS BITS. DIGITAL ADDRESS FOR DAC0 TO DAC7. DETERMINES WHICH DAC'S INPUT LATCH RECEIVES THE 8 BITS OF DATA IN THE NEXT BYTE. |
| ACK: | ACKNOWLEDGE BIT. THE MAX521 PULLS SDA LOW DURING THE 9TH CLOCK PULSE. |

*Figure 6. Command Byte*

Setting the PD bit high powers down the MAX521 following a STOP condition (Figure 8a). If a command byte with PD set high is followed by an output byte, the addressed DAC's input latch will be updated and the data will be transferred to the DAC's output latch following the STOP condition (Figure 8b). If the transmission's last command byte has PD high, the voltage outputs will not reflect the newly entered data because the DAC will enter power-down mode when the STOP condition is detected. When in power-down, the DAC outputs float. In this mode, the supply current is a maximum of 20µA. A command byte with the PD bit low returns the MAX521 to normal operation following a STOP condition, and the voltage outputs reflect the current output-latch contents (Figures 9a and 9b). Because each subsequent command byte overwrites the previous PD bit, only the last command byte of a transmission affects the MAX521's power-down state.

Setting the RST bit high clears all DAC input latches. The DAC outputs remain unchanged until a STOP condition is detected (Figure 10a). If a reset is issued, the following output byte is ignored. Subsequent pairs of command/output bytes overwrite the input latches (Figure 10b).

All changes made during a transmission affect the MAX521's outputs only when the transmission ends and a STOP has been recognized. The R0, R1, and R2 bits are reserved bits that must be set to zero.

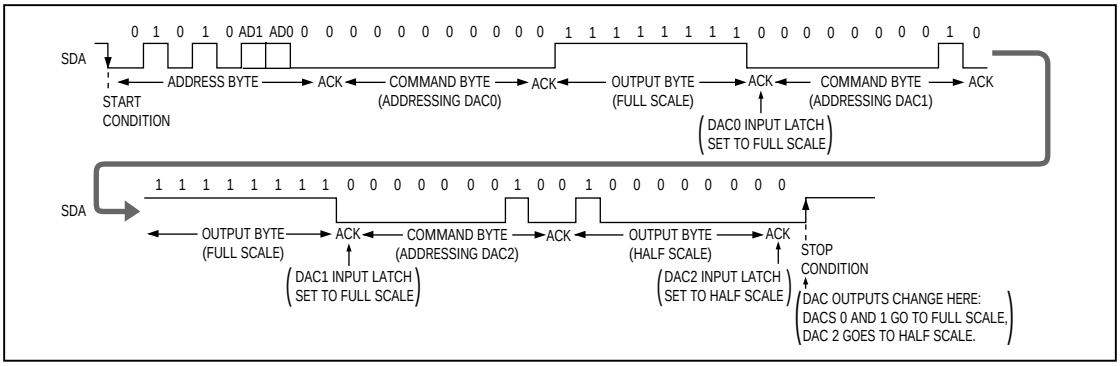



*Figure 7. Setting DAC Outputs*

# Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

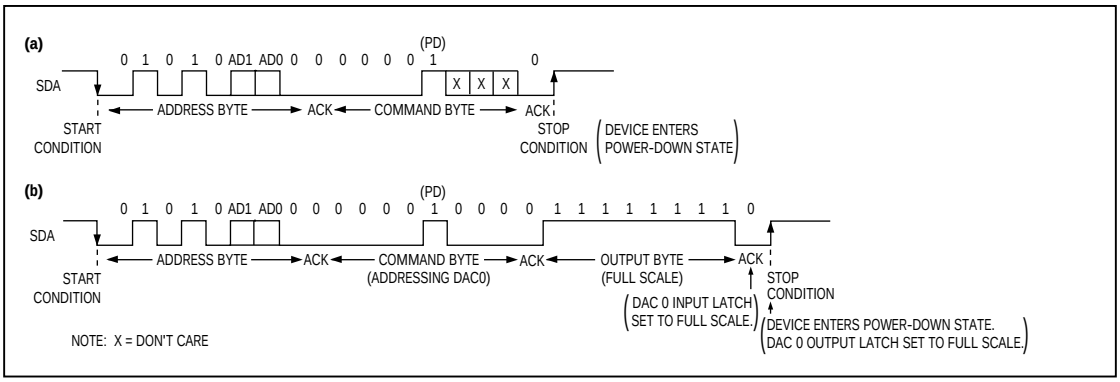



*Figure 8. Entering the Power-Down State*

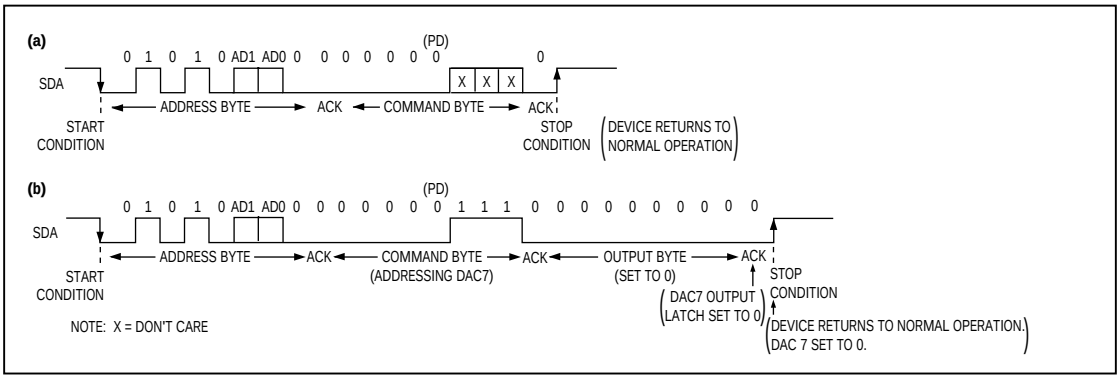



*Figure 9. Returning to Normal Operation from Power-Down*

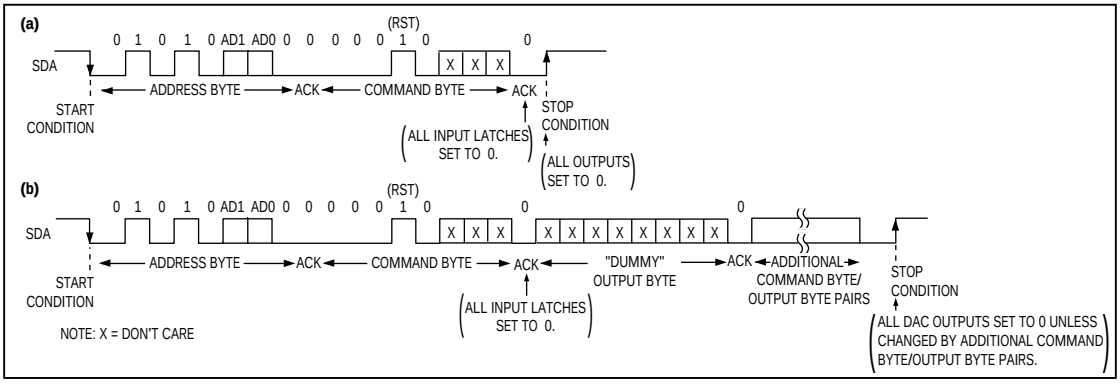



*Figure 10. Resetting DAC Outputs*

### *I²C Compatibility*

The MAX521 is fully compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain which pulls the data line low during the 9th clock pulse. Figure 11 shows the MAX521 being used in a typical I²C application.

### *Additional START Conditions*

It is possible to interrupt a transmission to a MAX521 with a new START (repeated start) condition (perhaps addressing another device), which leaves the input latches with data that has not been transferred to the output latches (Figure 12). Only the currently addressed MAX521 will recognize a STOP condition and transfer data to its output latches. If the MAX521 is left with data in its input latches, the data can be transferred to the output latches the next time the device is addressed, as long as it receives at least one command byte and a STOP condition.

### *Early Stop Conditions*

The addressed MAX521 recognizes a STOP condition at any point in a transmission. If the STOP occurs during a command byte, all previous uninterrupted command and output byte pairs are accepted, the interrupted command byte is ignored, and the transmission ends (Figure 13a). If the STOP occurs during an output byte, all previous uninterrupted command and output byte pairs are accepted, the final command byte's PD and RST bits are accepted, the interrupted output byte is ignored, and the transmission ends (Figure 13b).

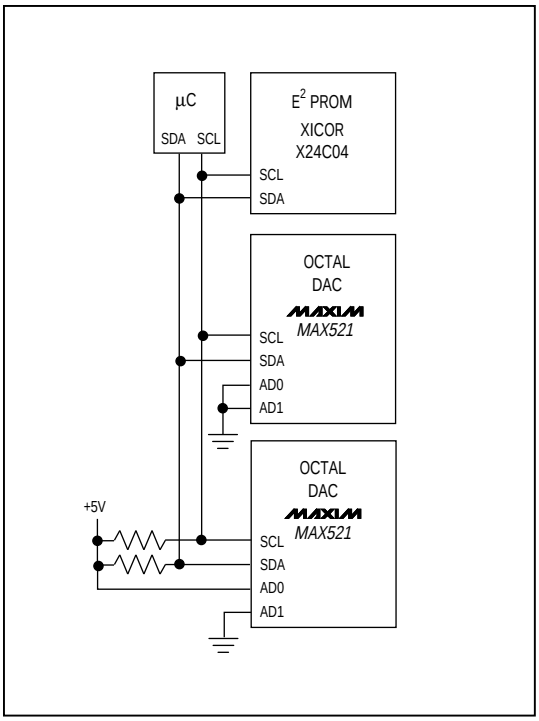



*Figure 11. MAX521 Used in a Typical I²C Application Circuit*

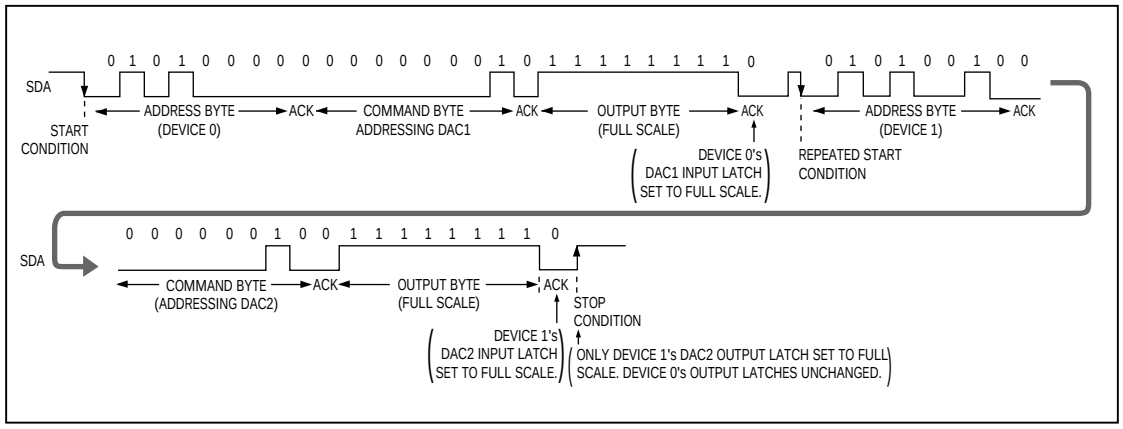



*Figure 12. Repeated START Conditions*

# Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

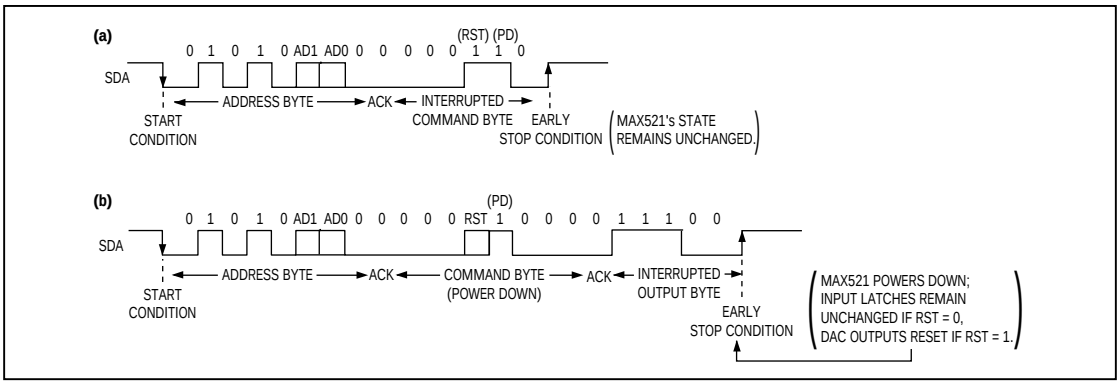



*Figure 13. Early STOP Conditions*

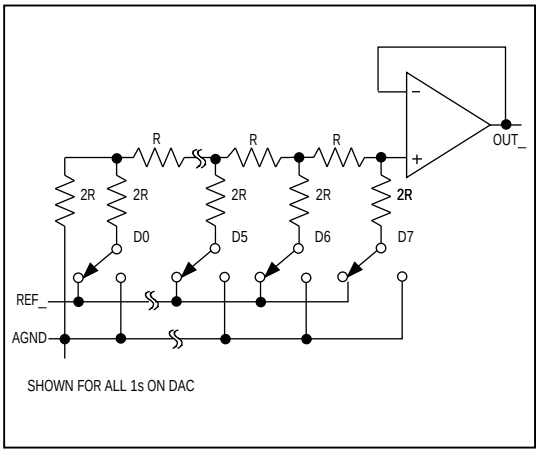



*Figure 14. DAC Simplified Circuit Diagram*

## Analog Section

### DAC Operation

The MAX521 contains eight matched voltage-output DACs. The DACs are inverted R-2R ladder networks that convert 8-bit digital words into equivalent analog output voltages in proportion to the applied reference voltages. DAC0–DAC3 each have separate reference inputs while DAC4–DAC7 all share a common reference input. Figure 14 shows a simplified diagram of one of the eight DACs.

### Reference Inputs

The MAX521 can be used for multiplying applications. The reference accepts a 0V to $V_{DD}$ voltage, both DC and AC signals. The voltage at each REF input sets the full-scale output voltage for its respective DAC(s). The reference voltage must be positive. The DAC's input impedance is code dependent, with the lowest value occurring when the input code is 55 hex or 0101 0101, and the maximum value occurring when the input code is 00 hex. Since the REF input resistance (RIN) is code dependent, it must be driven by a circuit with low output impedance (no more than RIN ÷ 2000) to maintain output linearity. The REF input capacitance is also code dependent, with the maximum value occurring at code FF hex (typically 120pF for REF4, and 30pF for REF0–REF3). The output voltage for any DAC can be represented by a digitally programmable voltage source as: $V_{OUT} = (N \times V_{REF}) / 256$, where N is the numerical value of the DAC's binary input code.

### Output Buffer Amplifiers

The MAX521 voltage outputs (OUT0–OUT7) are internally buffered precision unity-gain followers that slew up to 1V/µs. The outputs can swing from 0V to $V_{DD}$. With a 0V to 4V (or 4V to 0V) output transition, the amplifier outputs typically settle to 1/2LSB in 6µs when loaded with 10kΩ in parallel with 100pF. The buffer amplifiers are stable with any combination of resistive loads ≥2kΩ and capacitive loads ≤300pF.

The MAX521 is designed for unipolar-output, single-quadrant multiplication where the output voltages and the reference inputs are positive with respect to AGND. Table 1 shows the unipolar code.

**Table 1. Unipolar Code Table**

| DAC CONTENTS | ANALOG OUTPUT |
|---|---|
| 11111111 | $+ V_{REF}\left(\frac{255}{256}\right)$ |
| 10000001 | $+ V_{REF}\left(\frac{129}{256}\right)$ |
| 10000000 | $+ V_{REF}\left(\frac{128}{256}\right) = \frac{V_{REF}}{2}$ |
| 01111111 | $+ V_{REF}\left(\frac{127}{256}\right)$ |
| 00000001 | $+ V_{REF}\left(\frac{1}{256}\right)$ |
| 00000000 | 0V |

## Applications Information

### Power-Supply Bypassing and Ground Management

Bypass $V_{DD}$ with a 0.1µF capacitor, located as close to $V_{DD}$ and DGND as possible. The analog ground (AGND) and digital ground (DGND) pins should be connected in a "star" configuration to the highest quality ground available, which should be located as close to the MAX521 as possible.

Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Figure 15 shows the suggested PC board layout to minimize crosstalk

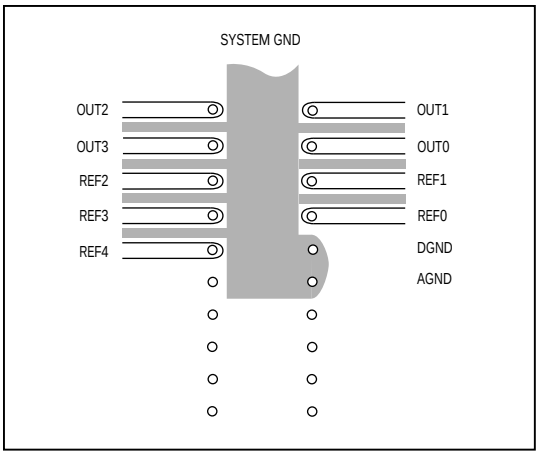



*Figure 15. PC Board Layout for Minimizing Crosstalk (bottom view, DIP package)*

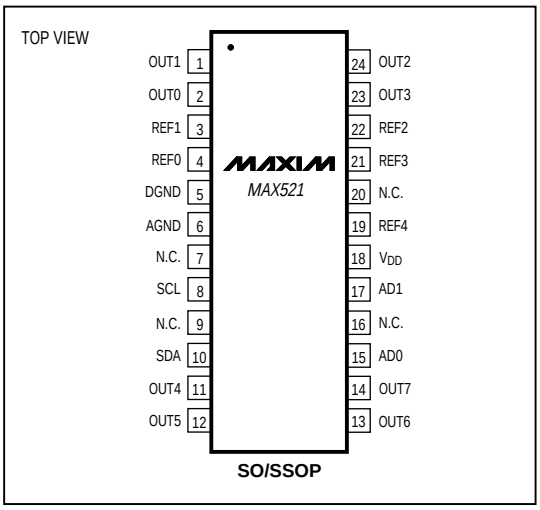
# Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs

## Ordering Information (continued)

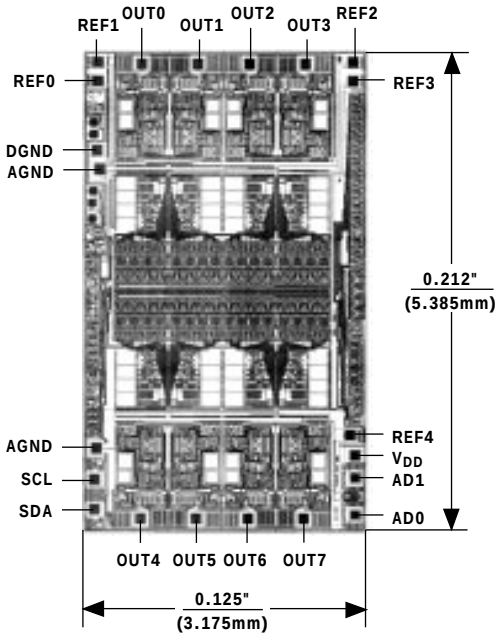
| PART | TEMP. RANGE | PIN-PACKAGE | TUE (LSB) |
|---|---|---|---|
| MAX521AEPP | -40°C to +85°C | 20 Plastic DIP | 1 |
| MAX521BEPP | -40°C to +85°C | 20 Plastic DIP | 2 |
| MAX521AEWG | -40°C to +85°C | 24 Wide SO | 1 |
| MAX521BEWG | -40°C to +85°C | 24 Wide SO | 2 |
| MAX521AEAG | -40°C to +85°C | 24 SSOP | 1 |
| MAX521BEAG | -40°C to +85°C | 24 SSOP | 2 |
| MAX521BMJP | -55°C to +125°C | 20 CERDIP** | 2 |

** Dice are specified at $T_A$ = +25°C, DC parameters only.*
***Contact factory for availability.*

## Pin Configurations (continued)

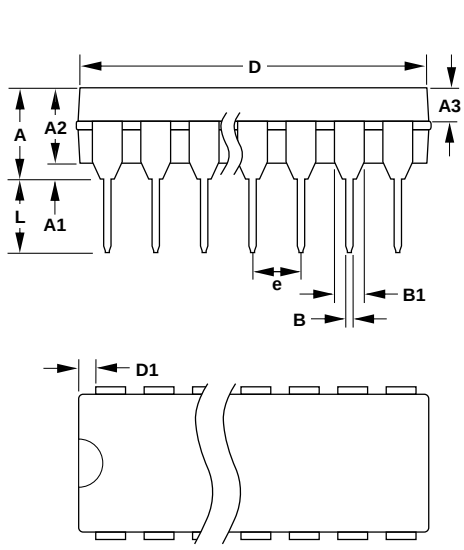



## Chip Topography




TRANSISTOR COUNT: 4518
SUBSTRATE CONNECTED TO $V_{DD}$

## Package Information

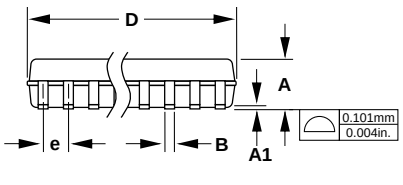



| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | – | 0.200 | – | 5.08 |
| A1 | 0.015 | – | 0.38 | – |
| A2 | 0.125 | 0.175 | 3.18 | 4.45 |
| A3 | 0.055 | 0.080 | 1.40 | 2.03 |
| B | 0.016 | 0.022 | 0.41 | 0.56 |
| B1 | 0.045 | 0.065 | 1.14 | 1.65 |
| C | 0.008 | 0.012 | 0.20 | 0.30 |
| D1 | 0.005 | 0.080 | 0.13 | 2.03 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 | – | 2.54 | – |
| eA | 0.300 | – | 7.62 | – |
| eB | – | 0.400 | – | 10.16 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |

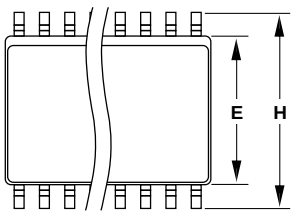
**Plastic DIP**
**PLASTIC**
**DUAL-IN-LINE**
**PACKAGE**
**(0.300 in.)**

| PKG. | DIM | PINS | INCHES | | MILLIMETERS | |
|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX |
| P | D | 8 | 0.348 | 0.390 | 8.84 | 9.91 |
| P | D | 14 | 0.735 | 0.765 | 18.67 | 19.43 |
| P | D | 16 | 0.745 | 0.765 | 18.92 | 19.43 |
| P | D | 18 | 0.885 | 0.915 | 22.48 | 23.24 |
| P | D | 20 | 1.015 | 1.045 | 25.78 | 26.54 |
| N | D | 24 | 1.14 | 1.265 | 28.96 | 32.13 |

21-0043A




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| A1 | 0.004 | 0.012 | 0.10 | 0.30 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| e | 0.050 | | 1.27 | |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

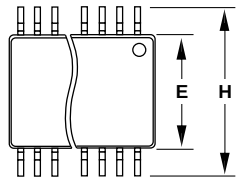


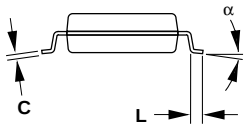

**Wide SO**
**SMALL-OUTLINE**
**PACKAGE**
**(0.300 in.)**

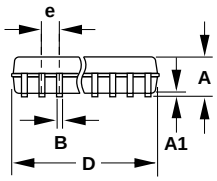
| DIM | PINS | INCHES | | MILLIMETERS | |
|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX |
| D | 16 | 0.398 | 0.413 | 10.10 | 10.50 |
| D | 18 | 0.447 | 0.463 | 11.35 | 11.75 |
| D | 20 | 0.496 | 0.512 | 12.60 | 13.00 |
| D | 24 | 0.598 | 0.614 | 15.20 | 15.60 |
| D | 28 | 0.697 | 0.713 | 17.70 | 18.10 |

21-0042A

## Package Information (continued)




**SSOP**
**SHRINK**
**SMALL-OUTLINE**
**PACKAGE**

| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.068 | 0.078 | 1.73 | 1.99 |
| A1 | 0.002 | 0.008 | 0.05 | 0.21 |
| B | 0.010 | 0.015 | 0.25 | 0.38 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | SEE VARIATIONS | | | |
| E | 0.205 | 0.209 | 5.20 | 5.38 |
| e | 0.0256 BSC | | 0.65 BSC | |
| H | 0.301 | 0.311 | 7.65 | 7.90 |
| L | 0.025 | 0.037 | 0.63 | 0.95 |
| α | 0° | 8° | 0° | 8° |

| DIM | PINS | INCHES | | MILLIMETERS | |
|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX |
| D | 14 | 0.239 | 0.249 | 6.07 | 6.33 |
| D | 16 | 0.239 | 0.249 | 6.07 | 6.33 |
| D | 20 | 0.278 | 0.289 | 7.07 | 7.33 |
| D | 24 | 0.317 | 0.328 | 8.07 | 8.33 |
| D | 28 | 0.397 | 0.407 | 10.07 | 10.33 |

21-0056A