ETC5040 • ETC5040A

PCM MONOLITHIC FILTER

The ETC5040/ETC5040A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is fifth order elliptic low pass filter in series with a fourth order Chebychev high pass filter. It provides a flat response in the passband and rejection of signals below 200 Hz and above 3.4 kHz.

RECEIVE FILTER STAGE

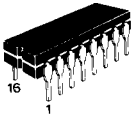
The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat pass-band response.

- Exceeds all D3/D4 and CCITT specifications
- + 5V, −5V power supplies
- Low power consumption :
  - 45 mW (600 Ω-0 dBm load)
  - 30 mW (power amps disabled)
- Power down mode : 0.5 mW
- 20 dB gain adjust range
- No external anti-aliasing components
- Sin x/x correction in receive filter
- 50/60 Hz rejection in transmit filter
- TTL and CMOS compatible logic
- All inputs protected against static discharge due to handling

CMOS

PCM
MONOLITHIC FILTER

CASE



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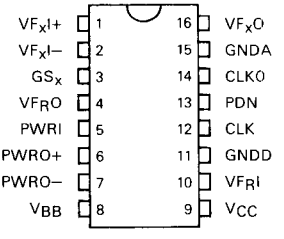
CERDIP PACKAGE

PIN ASSIGNMENT



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BLOCK DIAGRAM

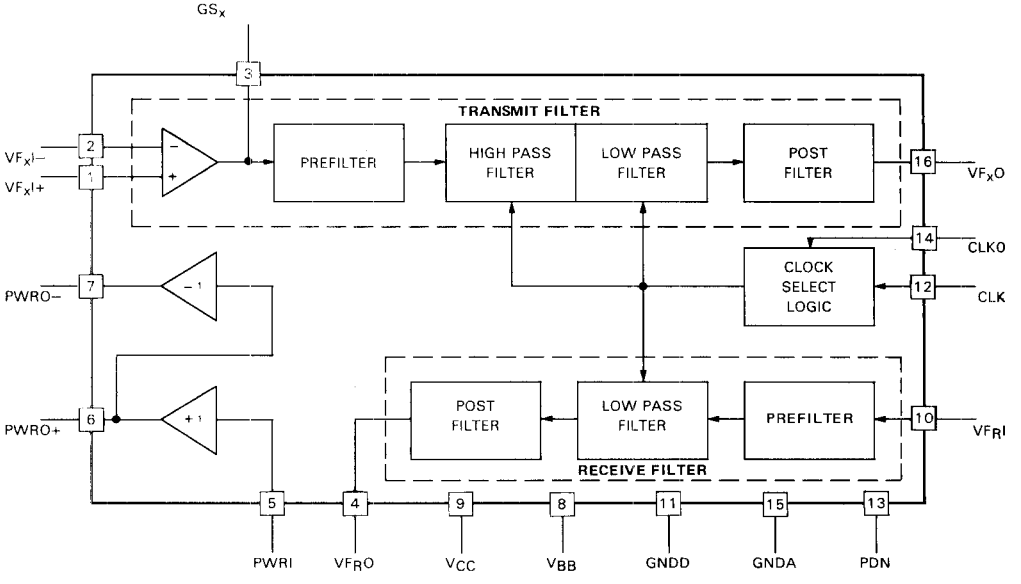


FIGURE 1

PIN DESCRIPTION

Name	Pin Type	N°	Description
VF_XI+	I	1	The non-inverting input to the transmit filter stage
VF_XI-	I	2	The inverting input to the transmit filter stage
GS_X	O	3	The output used for gain adjustments of the transmit filter
VF_RO	O	4	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
PWRI	I	5	The input to the receive filter differential power amplifier.
PWRO+	O	6	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
PWRO–	O	7	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
V_{BB}	S	8	The negative power supply pin. Recommended input is –5 V.
V_{CC}	S	9	The positive power supply pin. The recommended input is 5 V.
VF_RI	I	10	The input pin for the receive filter stage.
GNDD	GND	11	Digital ground input pin. All digital signals are referenced to this pin.
CLK	I	12	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
PDN	I	13	The input pin used to power down the ETC5040/ETC5040A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
CLKO	I	14	This input pin selects internal counters in accordance with the CLK input clock frequency : **CLK** **Connect CLKO to:** 2048 kHz V_{CC} 1544 kHz GNDD 1536 kHz V_{BB} An internal pull-up is provided.
GNDA	GND	15	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
VF_XO	O	16	The output of the transmit filter stage.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	±7	V
Input voltage	V_{in}	±7	V
Operating temperature range	T_A	−25°C to +125 °C	°C
Storage temperature	T_{stg}	−65°C to + 150°C	°C
Power dissipation	P_D	1/package	W
Output short-circuit duration		continuous	
Lead temperature		300	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, V_{BB} = − 5.0V ± 5%, clock frequency is 2.048 MHz
Typical parameters are specified at T_A = + 25°C, V_{CC} = 5.0V, V_{BB} = − 5.0 V (Unless otherwise specified)
Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

POWER DISSIPATION

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} standby current (PDN = V_{DD}, power down mode)	I_{CC0}	–	50	100	µA
V_{BB} standby current (PDN = V_{DD}, power down mode)	I_{BB0}	–	−50	−100	µA
V_{CC} operating current (PWRI = V_{BB}, power amp inactive)	I_{CC1}	–	3.0	4.0	mA
V_{BB} operating current (PWRI = V_{BB}, power amp inactive)	I_{BB1}	–	−3.0	−4.0	mA
V_{CC} operating current (Note 1)	I_{CC2}	–	4.6	6.4	mA
V_{BB} operating current (Note 1)	I_{BB2}	–	−4.6	−6.4	mA

DIGITAL INTERFACE

Characteristic	Symbol	Min	Typ	Max	Unit
Input current, CLK (0 V ≦ V_{IN} ≦ V_{CC})	I_{INC}	−10	–	10	µA
Input current, PDN (0 V ≦ V_{IN} ≦ V_{CC}−2 V)	I_{INP}	−100	–	–	µA
Input current, CLKO (V_{BB} ≦ V_{IN} ≦ V_{CC}−2 V)	I_{INO}	−10	–	−0.1	µA
Input low voltage, CLK, PDN	V_{IL}	0	–	0.8	V
Input high voltage, CLK, PDN	V_{IH}	2.2	–	V_{CC}	V
Input low voltage, CLKO	V_{ILO}	V_{BB}	–	V_{BB}+0.5	V
Input intermediate voltage, CLKO	V_{IIO}	−0.8	–	0.8	V
Input high voltage, CLKO	V_{IHO}	V_{CC}−0.5	–	V_{CC}	V

TRANSMIT INPUT AMP. OP.

Characteristic	Symbol	Min	Typ	Max	Unit
Input leakage current, VF_xI (V_{BB} ≦ VF_xI ≦ V_{CC})	IB_xI	−100	–	100	nA
Input resistance VF_xI (V_{BB} ≦ VF_xI ≦ V_{CC})	RI_xI	10	–	–	MΩ
Input offset voltage, VF_xI (−2.5 V ≦ V_{IN} ≦ +2.5 V)	VOS_xI	−20	–	20	mV
Common-mode range, VF_xI	V_{CM}	−2.5	–	2.5	V
Common-mode rejection ratio (−2.5V ≦ V_{IN} ≦ 2.5 V)	CMRR	60	–	–	dB
Power supply rejection of V_{CC} or V_{BB}	PSRR	60	–	–	dB
Open loop output resistance GS_x	R_{OL}	–	1	–	kΩ
Minimum load resistance, GS_x	R_L	10	–	–	kΩ
Maximum load capacitance, GS_x	C_L	–	–	100	pF
Output voltage swing, GS_x (R_L ≧ 10 kΩ)	VO_xI	± 2.5	–	–	V
Open loop voltage gain, GS_x (R_I ≧ 10 kΩ)	A_{VOL}	5,000	–	–	V/V
Open loop unity gain bandwidth, GS_x	F_C	–	2	–	MHz

AC ELECTRICAL CHARACTERISTICS

T_A = + 25° C. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. (Unless otherwise specified).

TRANSMIT FILTER (Note 2)

Characteristic		Symbol	Min	Typ	Max	Unit
Minimum load resistance		RL_X				kΩ
$-2.5\ V < V_{out} < +2.5\ V$			3	–	–	
$-3.2\ V < V_{out} < +3.2\ V$			10	–	–	
Load capacitance, VF_XO		CL_X	–	–	100	pF
Output resistance, VF_XO			–	1	3	Ω
V_{CC} power supply rejection VF_XI (f=1kHz, VF_XI+ = 0 Vrms)		PSRR1	30	–	–	dB
V_{BB} power supply rejection, VF_XO. (Same as above)		PSRR2	35	–	–	dB
Absolute gain (f = 1 kHz)		GA_X				dB
	ETC5040A		2.9	3.0	3.1	
	ETC5040		2.875	3.0	3.125	
Gain relative to GA_X		GR_X				dB
Below 50 Hz			–	–	−35	
50 Hz			–	−41	−35	
60 Hz			–	−35	−30	
200 Hz	ETC5040A		−1,5	–	0	
	ETC5040		−1.5	–	0.05	
300 Hz to 3 kHz	ETC5040A		−0.125	–	0.125	
	ETC5040		−0.15	–	0.15	
3.3 kHz	ETC5040A		−0.35	–	0.03	
	ETC5040		−0.35	–	0.125	
3.4 kHz			−0.70	–	−0.1	
4.0 kHz			–	−15	−14	
4.6 kHz and above			–	–	−32	
Absolute delay at 1 kHz		DA_X	–	–	230	µs
Differential envelope delay from 1 kHz to 2.6 kHz			–	–	60	µs
Single frequency distortion products		DP_X1	–	–	−48	dB
Distortion at maximum signal level		DP_X2				dB
1.6 Vrms, 1kHz signal applied to VF_XI+, gain = 20 dB, R_L = 10 kΩ			–	–	−45	
Total C message noise at VF_XO		NC_X1	–	2	5	dBrnc0
Total C message noise at VF_XO		NC_X2				dBrnc0
Gain setting 0p Amp at 20 dB, non inverting, note 3, $0°C \leq T_A \leq +70°C$			–	3	6	
Temperature coefficient of 1 kHz gain		GA_XT	–	0.0004	–	dB/°C
Supply voltage coefficient of 1 kHz gain		GA_XS	–	0.01	–	dB/V
Crosstalk, receive to transmit 20 log $\frac{VF_XO}{VF_RO}$		CTR_X				dB
Receive filter output = 2.2 Vrms,						
VF_XI+ = 0 Vrms, f= 0.2 kHz to 3.4 kHz, measure VF_XO			–	–	−70	
Gaintracking relative to GA_X		GR_XL				dB
Output level = + 3 dBm0			−0.1	–	0.1	
+ 2 dBm0 to − 40 dBm0			−0.05	–	0.05	
− 40 dBm0 to − 55 dBm0			−0.1	–	0.1	

AC ELECTRICAL CHARACTERISTICS (Continued)

T_A = + 25° C. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. (Unless otherwise specified).

RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter within an input signal level of 1.54 Vrms).

Characteristic	Symbol	Min	Typ	Max	Unit
Input leakage current, VF_RI (−3.2 V ≤ V_{IN} ≤ 3.2 V)	IB_R	−100	–	100	nA
Input resistance, VF_RI	RI_R	10	–	–	MΩ
Output resistance, VF_RO	RO_R	–	1	3	Ω
Load capacitance, VF_RO	CL_R	–	–	100	pF
Load resistance, VF_RO	RL_R	10	–	–	kΩ
Power supply rejection of V_{CC} or V_{BB} (VF_RO VF_RI connected to GNDA, f = 1 kHz)	PSRR3	35	–	–	dB
Output DC offset, VF_RO (VF_RI connected to GNDA)	VOS_RO	− 200	–	+ 200	mV
Absolute gain (f = 1 kHz)	GA_R				dB
ETC5040A		−0.1	0	0.1	
ETC5040		−0.125	0	0.125	
Gain relative to gain at 1 kHz below 300 Hz	GR_R	–	–	0.125	dB
300 Hz to 3.0 kHz ETC5040A		− 0.125	–	0.125	
3.3 kHz ETC5040A		− 0.35	–	0.03	
3.4 kHz		− 0.70	–	− 0.1	
4.0 kHz		–	–	− 14	
4.6 kHz and above		–	–	− 32	
Absolute delay at 1 kHz	DA_R	–	–	100	µs
Differential envelope delay 1 kHz to 2.6 kHz	DD_R	–	–	100	µs
Single frequency distortion products (f = 1 kHz)	DP_R1	–	–	−48	dB
Distortion at maximum signal level 2.2 Vrms input to sin x/x filter, f = 1 kHz, R_L = 10 kΩ	DP_R2	–	–	−45	dB
Total C-message noise at VF_RO	NC_R	–	3	5	dBrnc0
Temperature coefficient of 1 kHz gain	GA_RT	–	0.0004	–	dB/°C
Supply voltage coefficient of 1 kHz gain	GA_RS	–	0.01	–	dB/V
Crosstalk, transmit to receive 20 log $\frac{VF_RO}{VF_XO}$ (Transmit filter output = 2.2 Vrms, VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz, measure VF_RO)	CT_{XR}	–	−80	−70	dB
Gaintraking relative to GA_R	GR_RL				dB
Output level = 3 dBm0		−0.1	–	0.1	
+ 2 dBm0 to − 40 dBm0		−0.05	–	0.05	
− 40 dBm0 to 55 dBm0		−0.1	–	0.1	

AC ELECTRICAL CHARACTERISTICS (Continued)

RECEIVE OUTPUT POWER AMPLIFIER

Characteristic	Symbol	Min	Typ	Max	Unit
Input leakage current, PWRI ($-3.2\ V \leq V_{IN} \leq 3.2\ V$)	IBP	0.1	–	3	µA
Input resistance, PWRI	RIP	10	–	–	MΩ
Output resistance, PWRO+, PWRO – (amplifiers active)	ROP1	–	1	–	Ω
Load capacitance, PWRO+, PWRO–	CLP	–	–	500	pF
Gain, PWRI to PWRO+ (R_L = 600 Ω connected between)	GAp+	–	1	–	V/V
Gain, PWRI to PWRO– PWRO + and PWRO –, input, level = 0 dBm0 (Note 4)	GAp–	– –	–1 –	– –	V/V
Gaintraking relative to 0dBm0 output level V = 2.05 Vrms, R_L = 600 Ω (Notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (Notes 4, 5)	GRpL	 –0.1 –0.1	 – –	 0.1 0.1	dB
Signal/distortion V = 2.05 Vrms, R_L = 600 Ω (Notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (Notes 4, 5)	S/Dp	 – –	 – –	 –45 –45	dB
Output DC offset, PWRO+, PWRO– (PWRI connected to GNDA)	VOSP	–50	–	50	mV
Power supply rejection of V_{CC} or V_{BB} (PWRI connected to GNDA)	PSRR5	45	–	–	dB

Note 1. Maximum power consumption depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600 Ω connected from PWRO+ PWRO

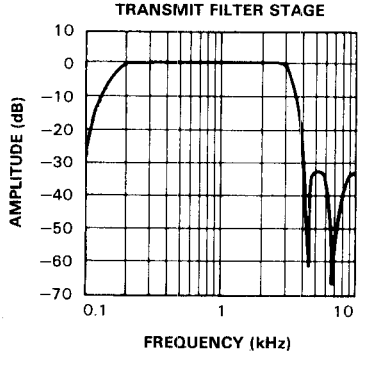
Note 2. Transmit filter input op amp set to the non inverting unity gain mode, with VF_XI+ = 1.1 Vrms, unless otherwise noted

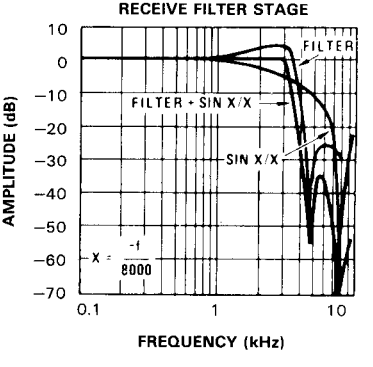
Note 3. The 0 dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter

Note 4. The 0 dBm0 level for the power amplifiers is load dependent. For R_L = – 600 Ω to GNDA, the 0 dBm0 level is 1.43 Vrms measured at the amplifier output. For R_L = 300 Ω the 0 dBm0 level is 1.22 Vrms.

Note 5. VF_RO connected to PWRI, input signal applied to VF_RI

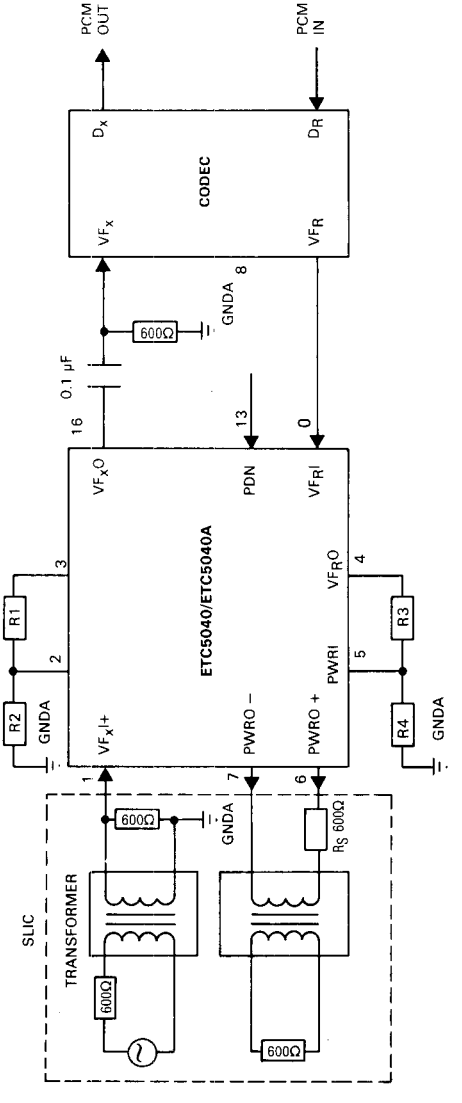
TYPICAL PERFORMANCE CHARACTERISTICS





INTERFACE

Circuit for CODEC



Note 1 : Transmit voltage gain = $\frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3 dB gain) (R1 + R2 ≧ 10 kΩ)

Note 2 : Receive gain = $\frac{R4}{R3 + R4}$

(R3 + R4 ≧ 10 kΩ)

Note 3 : In the configuration shown, the receive filter power amplifiers will drive a 600 Ω T to R termination to a signal level of 8.5 dBm. An alternative arrangement using a transformer winding ratio equivalent to 1.414.1 and 300 Ω resistor R_S, will provide a maximum signal level of 10 dBm across 600 Ω termination impedance.

FIGURE 2

FUNCTIONAL DESCRIPTION

The ETC 5040/ETC 5040A monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (figure 1). A brief description of the circuit operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance greater than 10 MΩ, a voltage gain of greater than 10.000, low power consumption (less than 3 mW), high power supply rejection, and is capable of driving a 10 kΩ load parallel with up to 25 pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20 dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200 Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40 dB. The output of the transmit filter is capable of driving a ± 3.2 V peak to peak signal into a 10 kΩ load in parallel with up to 25 pF.

Receive filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive filter power amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (figure 2). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10 mW-20 mW depending on output signal amplitude.

Power down control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1 mW and turn the power amplifier outputs into high impedance state.

Frequency divider and select logic circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic.

A frequency select circuit is provided to allow the filter to operate with 2.048 MHz, 1.544 MHz or 1.536 MHz clock frequen-cies. By connecting the frequency select pin CLKO (pin 14) to V_{CC}, a 2.048 MHz clock input frequency is selected. Digital ground selects 1.544 MHz and V_{BB} selects 1.536 MHz.

APPLICATIONS INFORMATION

Gain adjust

Figure 2 shows the signal path interconnections between the ETC5040/ETC5040A and single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

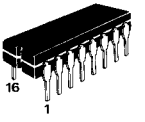
Optimum noise and distortion performance will be obtained from the ETC5040/ETC5040A filter when operated with system peak overload voltages of ± 2.5 V to ± 3.2 V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the ETC5040/ETC5040A filter can be used with CODEC which has a 5.5 V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

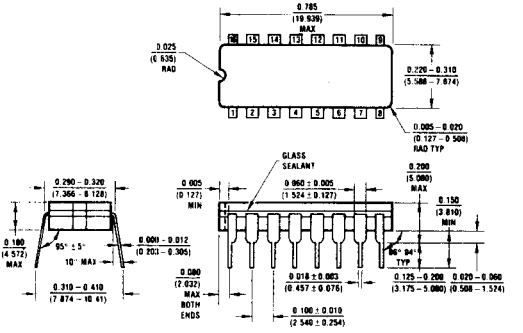
Board layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies.

Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between the GNDA traces of adjacent filters and CODECs.



J SUFFIX
CERDIP PACKAGE



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