

March 1997

Programmable Interrupt Controller (PIC)

Features

- Compatible with CDP1800 Series
- Programmable Long Branch Vector Address and Vector Interval
- 8 Levels of Interrupt Per Chip
- Easily Expandable
- Latched Interrupt Requests
- Hard Wired Interrupt Priorities
- Memory Mapped
- Multiple Chip Select Inputs to Minimize Address Space Requirements

Description

The CDP1877 and CDP1877C are programmable 8-level interrupt controllers designed for use in CDP1800 series microprocessor systems. They provide added versatility by extending the number of permissible interrupts from 1 to N in increments of 8.

When a high to low transition occurs on any of the PIC interrupt lines ($\overline{IR0}$ to $\overline{IR7}$), it will be latched and, unless the request is masked, it will cause the $\overline{INTERRUPT}$ line on the PIC and consequently the $\overline{INTERRUPT}$ input on the CPU to go low.

The CPU accesses the PIC by having interrupt vector register R(1) loaded with the memory address of the PIC. After the interrupt S3 cycle, this register value will appear at the CPU address bus, causing the CPU to fetch an instruction from the PIC. This fetch cycle clears the interrupt request latch bit to accept a new high-to-low transition, and also causes the PIC to issue a long branch instruction (CO) followed by the preprogrammed vector address written into the PIC's address registers, causing the CPU to branch to the address corresponding to the highest priority active interrupt request.

If no other unmasked interrupts are pending, the $\overline{INTERRUPT}$ output of the PIC will return high. When an interrupt is requested on a masked interrupt line, it will be latched but it will not cause the PIC $\overline{INTERRUPT}$ output to go low. All pending interrupts, masked and unmasked, will be indicated by a "1" in the corresponding bit of the status register. Reading of the status register will clear all pending interrupt request latches.

Several PICs can be cascaded together by connecting the $\overline{INTERRUPT}$ output of one chip to the $\overline{CASCADE}$ input of another. Each cascaded PIC provides 8 additional interrupt levels to the system. The number of units cascaded depends on the amount of memory space and the extent of the address decoding in the system.

Interrupts are prioritized in descending order; $\overline{IR7}$ has the highest and $\overline{IR0}$ has the lowest priority.

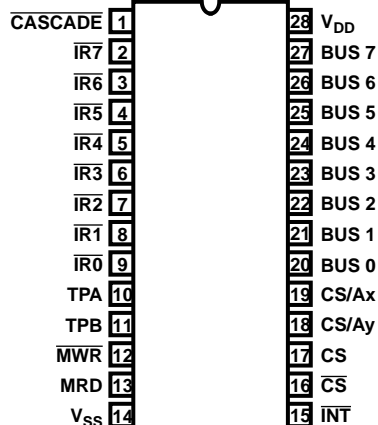
The CDP1877 and CDP1877C are functionally identical. They differ in that the CDP1877 has a recommended operating voltage range of 4V to 10.5V, and the CDP1877C has a recommended operating voltage range of 4V to 6.5V.

Ordering Information

| PACKAGE | TEMP. RANGE | 5V | 10V | PKG. NO. |
|---------|----------------|-----------|----------|----------|
| PDIP | -40°C to +85°C | CDP1877CE | CDP1877E | E28.6 |

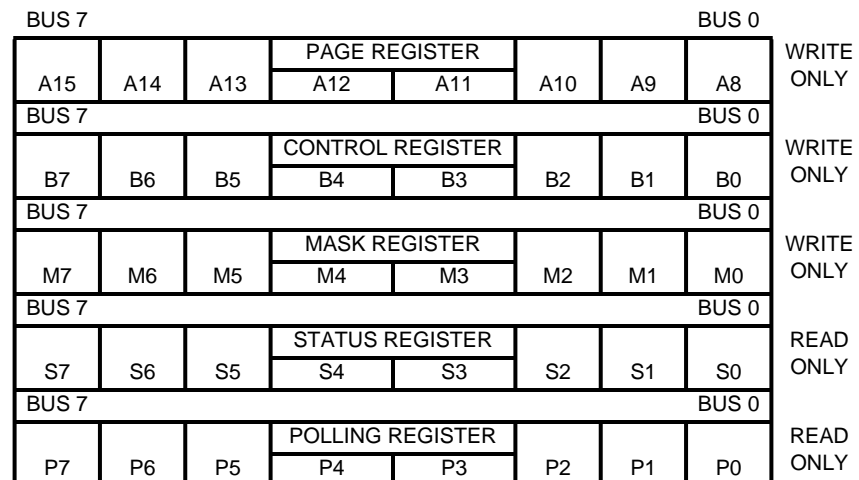
Pinout

CDP1877, CDP1877C (PDIP)
TOP VIEW



Programming Model

PROGRAMMABLE INTERRUPT CONTROLLER (PIC)



CDP1877, CDP1877C

Absolute Maximum Ratings

| | |
|---|--------------------------|
| DC Supply-Voltage Range, (V_{DD}) (All Voltages Referenced to V_{SS} Terminal) | |
| CDP1877 | -0.5V to +11V |
| CDP1877C | -0.5V to +7V |
| Input Voltage Range, All Inputs | -0.5V to $V_{DD} + 0.5V$ |
| DC Input Current, Any One Input | $\pm 10mA$ |

Thermal Information

| | |
|---|-------------------------------------|
| Thermal Resistance (Typical) | θ_{JA} ($^{\circ}C/W$) |
| PDIP Package | 55 |
| Device Dissipation Per Output Transistor | |
| T_A = Full Package Temperature Range (All Package Types) | 100mW |
| Operating Temperature Range (T_A) | |
| Package Type E | -40 $^{\circ}C$ to +85 $^{\circ}C$ |
| Storage Temperature Range (T_{STG}) | -65 $^{\circ}C$ to +150 $^{\circ}C$ |
| Lead Temperature (During Soldering) | |
| At distance 1/16 \pm 1/32 In. (1.59 \pm 0.79mm) | |
| from case for 10s max | +265 $^{\circ}C$ |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications At $T_A = -40$ to +85 $^{\circ}C$, $V_{DD} \pm 5\%$, Unless Otherwise Specified

| PARAMETER | | CONDITIONS | | | LIMITS | | | | | | UNITS |
|------------------------------------|------------|--------------|-----------------|-----------------|---------|----------------|----------|----------|----------------|---------|---------|
| | | V_O (V) | V_{IN} (V) | V_{DD} (V) | CDP1877 | | | CDP1877C | | | |
| | | | | | MIN | (NOTE1) TYP | MAX | MIN | (NOTE1) TYP | MAX | |
| Quiescent Device Current | I_{DD} | - | 0, 5 | 5 | - | 0.01 | 50 | - | 0.02 | 200 | μA |
| | | - | 0, 10 | 10 | - | 1 | 200 | - | - | - | μA |
| Output Low Drive (Sink) Current | I_{OL} | 0.4 | 0, 5 | 5 | 1.6 | 3.2 | - | 1.6 | 3.2 | - | mA |
| | | 0.5 | 0, 10 | 10 | 2.6 | 5.2 | - | - | - | - | mA |
| Output High Drive (Source) Current | I_{OH} | 4.6 | 0, 5 | 5 | -1.15 | -2.3 | - | -1.15 | -2.3 | - | mA |
| | | 9.5 | 0, 10 | 10 | -2.6 | -5.2 | - | - | - | - | mA |
| Output Voltage Low Level (Note 2) | V_{OL} | - | 0, 5 | 5 | - | 0 | 0.1 | - | 0 | 0.1 | V |
| | | - | 0, 10 | 10 | - | 0 | 0.1 | - | - | - | V |
| Output Voltage High Level (Note 2) | V_{OH} | - | 0, 5 | 5 | 4.9 | 5 | - | 4.9 | 5 | - | V |
| | | - | 0, 10 | 10 | 9.9 | 10 | - | - | - | - | V |
| Input Low Voltage | V_{IL} | 0.5, 4.5 | - | 5 | - | - | 1.5 | - | - | 1.5 | V |
| | | 0.5, 9.5 | - | 10 | - | - | 3 | - | - | - | V |
| Input High Voltage | V_{IH} | 0.5, 4.5 | - | 5 | 3.5 | - | - | 3.5 | - | - | V |
| | | 0.5, 9.5 | - | 10 | 7 | - | - | - | - | - | V |
| Input Leakage Current | I_{IN} | Any Input | 0, 5 | 5 | - | - | ± 1 | - | - | ± 1 | μA |
| | | | 0, 10 | 10 | - | - | ± 2 | - | - | - | μA |
| Three-State Output Leakage Current | I_{OUT} | 0, 5 | 0, 5 | 5 | - | $\pm 10^{-4}$ | ± 1 | - | $\pm 10^{-4}$ | ± 1 | μA |
| | | 0, 10 | 0, 10 | 10 | - | $\pm 10^{-4}$ | ± 10 | - | - | - | μA |
| Operating Device Current (Note 3) | I_{OPER} | - | - | 5 | - | 0.5 | 1.0 | - | 0.5 | 1.0 | mA |
| | | - | - | 10 | - | 1.9 | 3.0 | - | - | - | mA |
| Input Capacitance | C_{IN} | - | - | - | - | 5 | 7.5 | - | 5 | 7.5 | pF |
| Output Capacitance | C_{OUT} | - | - | - | - | 10 | 15 | - | 10 | 15 | pF |

NOTES:

- Typical values are for $T_A = +25^{\circ}C$ and nominal V_{DD} .
- $I_{OL} = I_{OH} = 1\mu A$
- Operating current is measured under worst-case conditions in a 3.2MHz CDP1802A system, one PIC access per instruction cycle.

CDP1877, CDP1877C

Operating Conditions At T_A = Full package temperature range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

| PARAMETER | LIMITS | | | | UNITS |
|----------------------------|----------|----------|----------|----------|-------|
| | CDP1877 | | CDP1877C | | |
| | MIN | MAX | MIN | MAX | |
| DC Operating Voltage Range | 4 | 10.5 | 4 | 6.5 | V |
| Input Voltage Range | V_{SS} | V_{DD} | V_{SS} | V_{DD} | V |

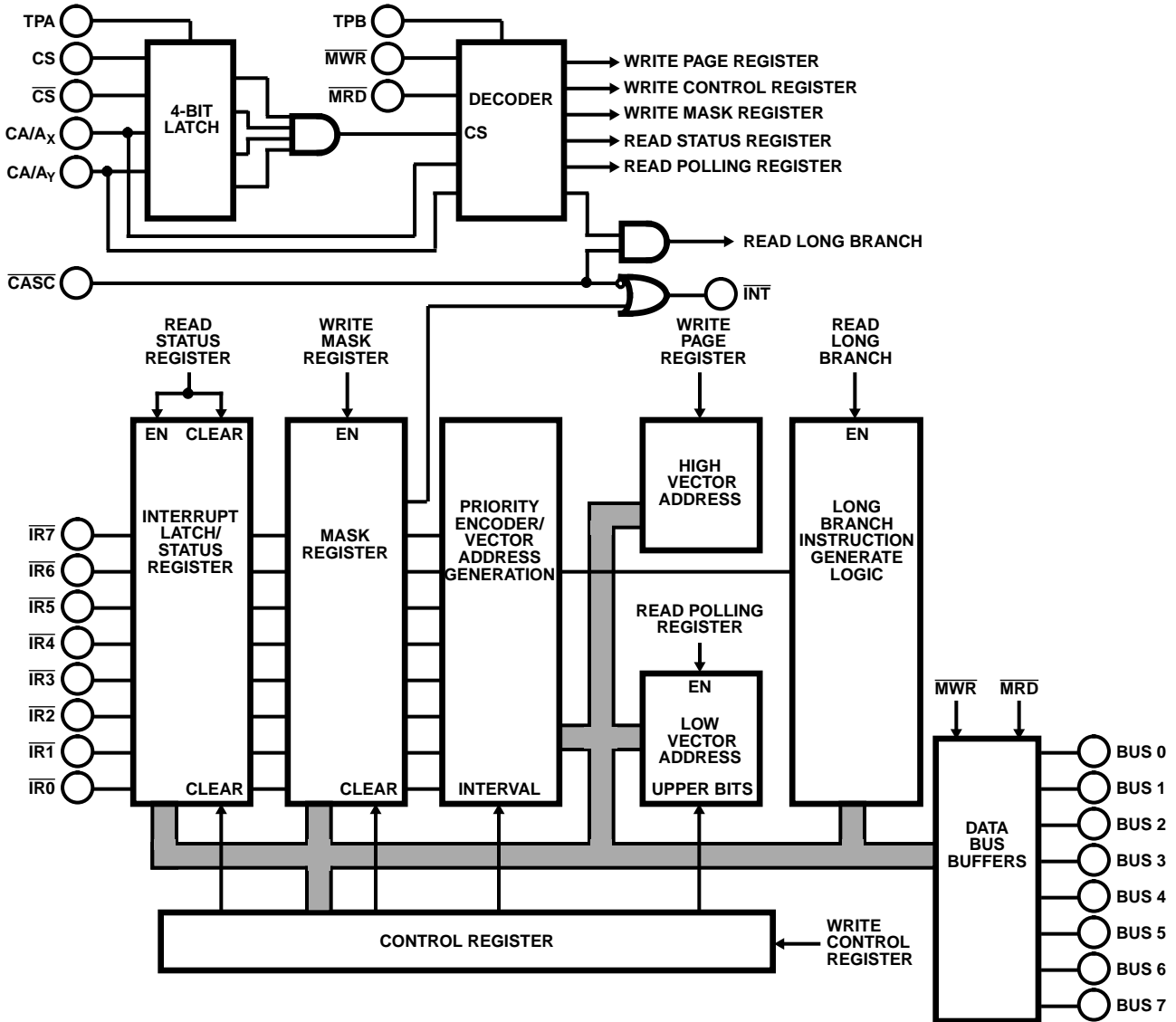


FIGURE 1. FUNCTIONAL DIAGRAM FOR CDP1877

Functional Definitions for CDP1877 and CDP1877C Terminals

| TERMINAL | USAGE | TYPE |
|---------------------------------------|--|---------------|
| V _{DD} - V _{SS} | Power | |
| BUS0 - BUS7 | Data Bus - Communicates Information to and from CPU | Bidirectional |
| IR ₀ - IR ₇ | Interrupt Request Lines | Input |
| INTERRUPT | Interrupt to CPU | Output |
| MRD, MWR | Read/Write Controls from CPU | Input |
| TPA, TPB | Timing Pulses from CPU | Input |
| CS, CS | Chip Selects, Enable Chip if Valid during TPA | Input |
| CS/A _x , CS/A _y | Used as a Chip Select during TPA and as a Register Address During Read/Write Operations | Input |
| CASCADE | Used for Cascading Several PIC Units. The INTERRUPT Output from a Higher Priority PIC can be Tied to this Input, or the Input can be Tied to V _{DD} if Cascading is Not Used. | Input |

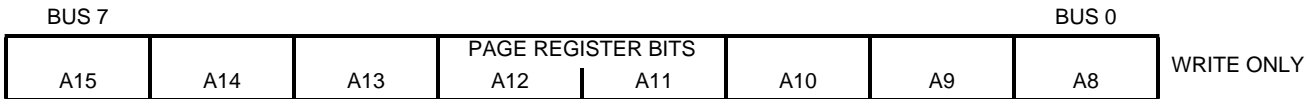
PIC Programming Model

INTERNAL REGISTERS

The PIC has three write-only programmable registers and two read-only registers.

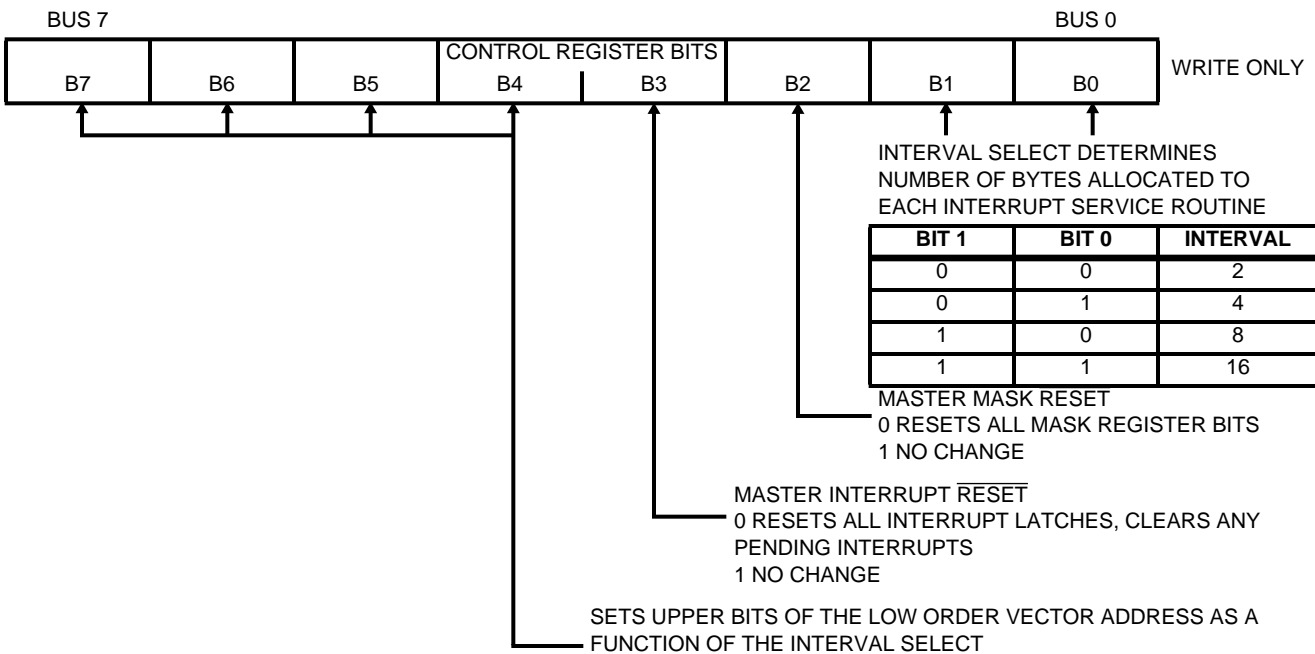
Page Register

This write only register contains the high order vector address the device will issue in response to an interrupt request. This high-order address will be the same for any of the 8 possible interrupt requests; thus, interrupt vectoring differs only in location within a specified page.



Control Register

The upper nibble of this write-only register contains the low order vector address the device will issue in response to an interrupt request. The lower nibble is used for a master interrupt reset, master mask reset and for interval select.



CDP1877, CDP1877C

The Low Order Vector Address will be set according to the table below:

| INTERVAL SELECTED NO. OF BYTES | LOW ADDRESS BITS | | | |
|--------------------------------|------------------|---------|---------|--------|
| | BIT B7 | BIT B6 | BIT B5 | BIT B4 |
| 2 | SETS A7 | SETS A6 | SETS A5 | SET A4 |
| 4 | SETS A7 | SETS A6 | SETS A5 | X |
| 8 | SETS A7 | SETS A6 | X | X |
| 16 | SETS A7 | X | X | X |

NOTES:

1. X = Don't Care
2. All Don't Care addresses and addresses A0-A3 are determined by interrupt request.

Mask Register

A "1" written into any location in this write only register will mask the corresponding interrupt request line. All interrupt inputs (except CASCADE) are maskable.

| | | | | | | | | |
|-------|----|----|--------------------|----|----|----|-------|------------|
| BUS 7 | | | | | | | BUS 0 | |
| M7 | M6 | M5 | MASK REGISTER BITS | | M2 | M1 | M0 | WRITE ONLY |
| | | | M4 | M3 | | | | |

Status Register

In this read only register a "1" will be present in the corresponding bit location for every masked or unmasked pending interrupt.

| | | | | | | | | |
|-------|----|----|----------------------|----|----|----|-------|-----------|
| BUS 7 | | | | | | | BUS 0 | |
| S7 | S6 | S5 | STATUS REGISTER BITS | | S2 | S1 | S0 | READ ONLY |
| | | | S4 | S3 | | | | |

Polling Register

This read only register provides the low order vector address and is used to identify the source of interrupt if a polling technique, rather than interrupt servicing, is used.

| | | | | | | | | |
|-------|----|----|-----------------------|----|----|----|-------|-----------|
| BUS 7 | | | | | | | BUS 0 | |
| P7 | P6 | P5 | POLLING REGISTER BITS | | P2 | P1 | P0 | READ ONLY |
| | | | P4 | P3 | | | | |

RESPONSE TO INTERRUPT (AFTER S3 CYCLE)

The PIC's response to interrogation by the CPU is always 3 bytes long, placed on the data bus in consecutive bytes in the following format:

First (Instruction) Byte:

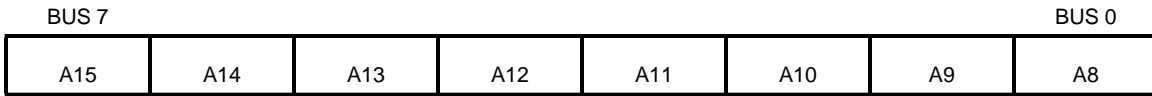
LONG BRANCH INSTRUCTION - CO (Hex)

| | | | | | | | |
|-------|---|---|---|---|---|---|-------|
| BUS 7 | | | | | | | BUS 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

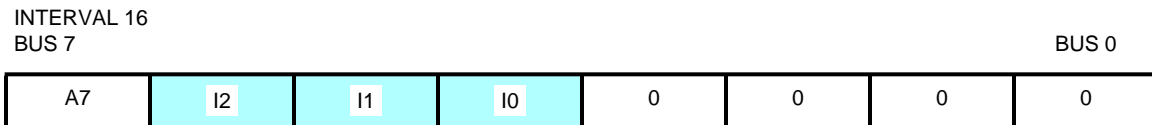
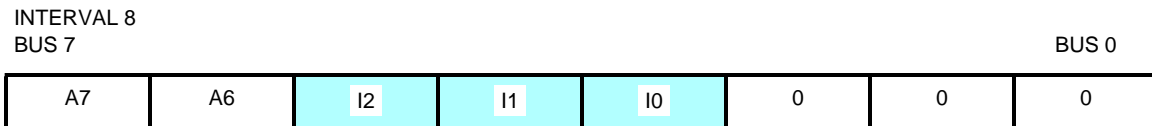
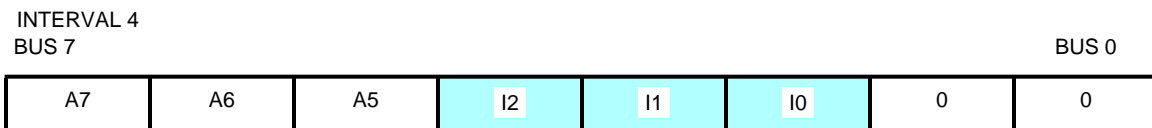
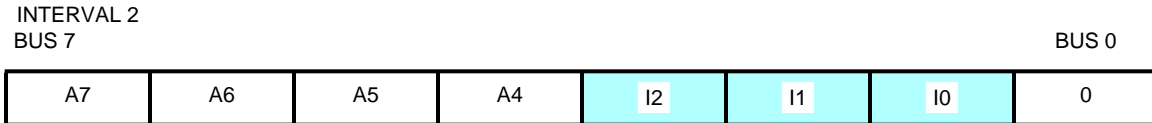
Second (High-Order Address) Byte

This byte is the High-Order vector Address that was written into the PIC's Page Register by the user. The PIC does not alter this value in any way.

High-Order Vector Address



Third (Low-Order Address) Bytes



Indicates active interrupt input number (binary 0 to 7).

Bits indicated by A_x ($x = 4$ to 7) are the same as programmed into the control register. All other bits are generated by the PIC.

REGISTER ADDRESSES

In order to read/write or obtain an interrupt vector from any PIC in the system, all chip selects (CS/A_x , CS/A_y , CS , \overline{CS}) must be valid during TPA.

CS/A_x and CS/A_y are multiplexed addresses; both must be high during TPA, and set according to this table during TPB to access the proper register.

| CS/A_x | CS/A_y | \overline{RD} | \overline{WR} | ACTION TAKEN |
|----------|----------|-----------------|-----------------|---|
| 1 | 0 | 0 | 1 | READ Long Branch instruction and vector for highest priority unmasked interrupt pending. |
| 1 | 0 | 1 | 0 | WRITE to Page Register |
| 0 | 1 | 1 | 0 | WRITE to Control Register |
| 0 | 0 | 0 | 1 | READ Status Register |
| 0 | 0 | 1 | 0 | WRITE to Mask Register |
| 0 | 1 | 0 | 1 | READ Polling Register (Used to identify INTERRUPT source if Polling technique rather than INTERRUPT service is used.) |
| 1 | 1 | X | X | Unused condition |

PIC Application Examples

Example 1 - Single PIC Application

Figure 2 shows all the connections required between CPU and PIC to handle eight levels of interrupt control.

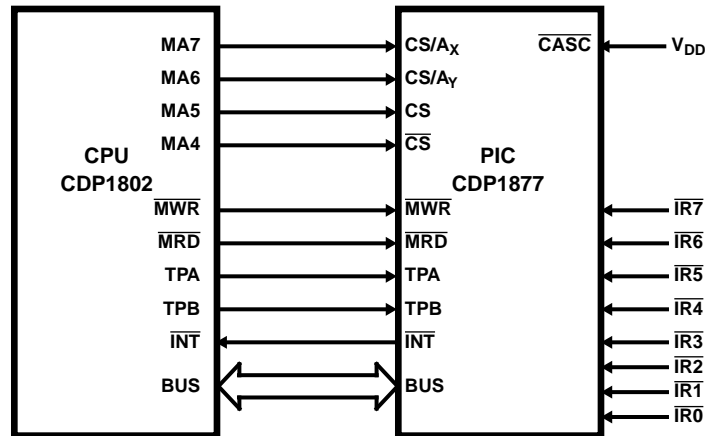


FIGURE 2. PIC AND CPU CONNECTION DIAGRAM

Programming

Programming the PIC consists of the following steps:

1. Disable interrupt at CPU
2. Reset Master Interrupt Bit, B3, of Control Register.
3. Write a "1" into the Interrupt Input bit location of the Mask Register, if masking is desired.
4. Write the High-Order Address byte into the Page Register.
5. Write the Low-Order Address and the vector interval into the Control Register.
6. Program R(1) of the CPU to point to the PIC so that the Long Branch instruction can be read from the PIC during the Interrupt Service routine.

Values for Example 1 with LOCATION 84E0 arbitrarily chosen as the Vector Address with interval of eight bytes, $\overline{IR4}$ pending, is shown in Table 1.

In deriving the above addresses, all Don't Care bits are assumed to be 0.

When an INTERRUPT ($\overline{IR4}$) is received by the CPU, it will address the PIC and will branch to the interrupt service routine.

The three bytes generated by the PIC will be:
 1st Byte = C0_H
 2nd Byte = 84_H
 3rd Byte = E0_H

TABLE 1. REGISTER ADDRESS VALUES

| REGISTER | REGISTER ADDRESS | OPERATION | DATA BYTE |
|---------------|------------------|-----------|-----------------|
| MASK | E000H | WRITE | 00 _H |
| CONTROL | E040H | WRITE | CE _H |
| PAGE | E080H | WRITE | 84 _H |
| STATUS | E000H | READ | 10 _H |
| POLLING | E040H | READ | E0 _H |
| R(1) (IN CPU) | E080H | - | - |

Example 2 - Multi-PIC Application

Figure 3 shows all the connections required between CPU and PIC's to handle sixteen levels of interrupt control.

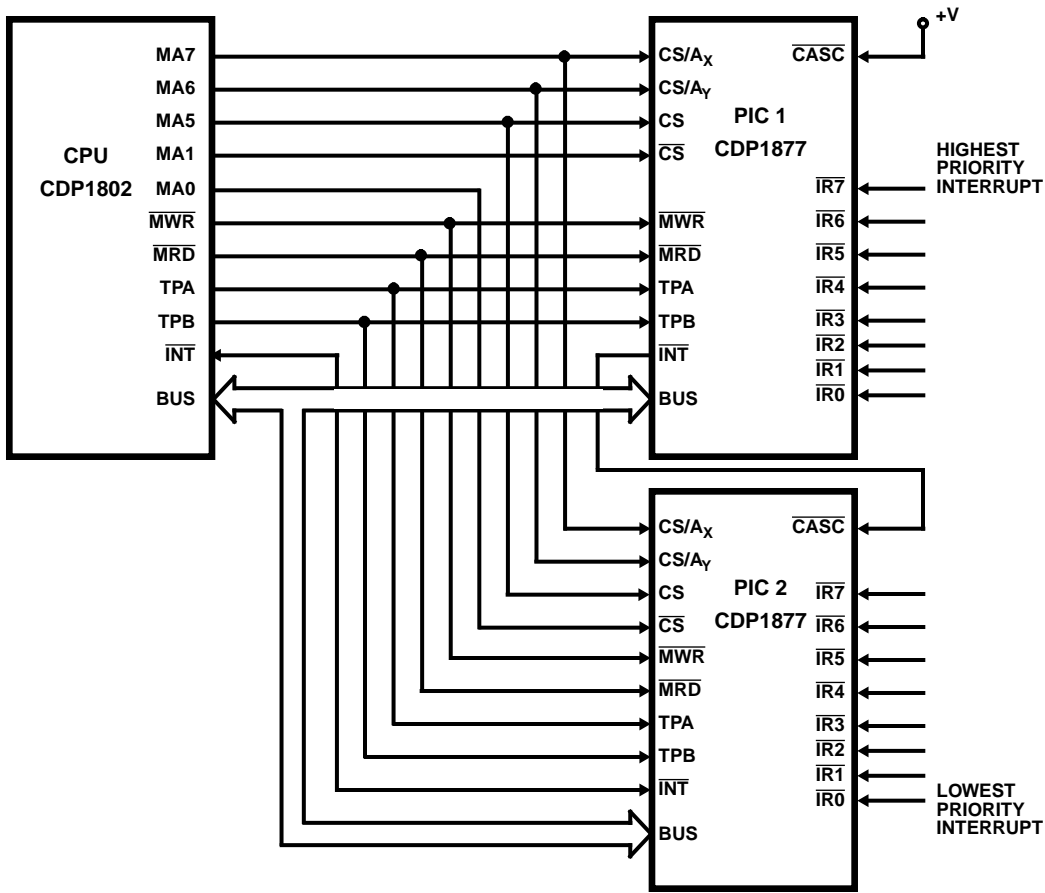


FIGURE 3. PICs AND CPU CONNECTION DIAGRAM

Register Address Assignments

The low-byte register address for any WRITE or READ operation is the same as shown in Table 1.

The High-Byte register differs for each PIC because of the linear addressing technique shown in the example:

- PIC 1 = 111XXX01 (E1_H for X = 0)
- PIC 2 = 111XXX10 (E2_H for X = 0)

The R(1) vector address is unchanged. This address will select both PICs simultaneously (R(1). 1 = 111XXX00 = E0_H). Internal CDP1877 logic controls which PIC will respond when an interrupt request is serviced.

Additional PIC Application Comments

The interval select options provide significant flexibility for interrupt routine memory allocations:

- The 2-byte interval allows one to dedicate a full page to interrupt servicing, with variable space between routines, by specifying indirect vectoring with 2-byte short branch instructions on the current page.

- The 4-byte interval allows for a 3-byte long branch to any location in memory where the interrupt service routine is located. The branch can be preceded by a Save Instruction to save previous contents of X and P on the stack.
- The 8-byte and 16-byte intervals allow enough space to perform a service routine without indirect vectoring. The amount of interval memory can be increased even further if all 8 INTERRUPTS are not required. Thus a 4-level interrupt system could use alternate \overline{IR} Inputs, and expand the interval to 16 and 32 bytes, respectively.
- The 4 Chip Selects allow one to conserve total allotted memory space to the PIC. For one chip, a total of 4 address lines could be used to select the device, mapping it into as little as 4-K of memory space. Note that this selection technique is the only one that allows the PIC to work properly in the system: I/O mapping cannot be used because the PIC must work within the CDP1800 interrupt structure to define the vector address. Decoded signals also will not work because the chip selects must be valid on the trailing edge of TPA.

CDP1877, CDP1877C

Dynamic Electrical Specifications At $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_R, t_F = 20\text{ns}$, $V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$, $C_L = 50\text{pF}$

| PARAMETER | | V_{DD} (V) | LIMITS | | | | | | UNITS |
|---|------------|-----------------|---------|-----------------|-----|----------|-----------------|-----|-------|
| | | | CDP1877 | | | CDP1877C | | | |
| | | | MIN | (NOTE 1) TYP | MAX | MIN | (NOTE 1) TYP | MAX | |
| Address to TPA Setup Time | t_{AS} | 5 | 60 | - | - | 60 | - | - | ns |
| | | 10 | 40 | - | - | - | - | - | ns |
| Address to TPA Hold Time | t_{AH} | 5 | 60 | - | - | 60 | - | - | ns |
| | | 10 | 40 | - | - | - | - | - | ns |
| Data Valid after TPB | t_{DTPB} | 5 | 370 | - | - | 370 | - | - | ns |
| | | 10 | 210 | 310 | - | - | - | - | ns |
| Data Hold Time from Write | t_{HW} | 5 | 30 | - | - | 30 | - | - | ns |
| | | 10 | 40 | - | - | - | - | - | ns |
| Address to Valid Data Access Time | t_{DR} | 5 | - | 340 | 490 | - | 340 | 490 | ns |
| | | 10 | - | 125 | 230 | - | - | - | ns |
| Data Setup Time to Write | t_{DSU} | 5 | 0 | - | - | 0 | - | - | ns |
| | | 10 | 0 | - | - | - | - | - | ns |
| Address Hold from TPB | t_{HTPB} | 5 | 80 | - | - | 80 | - | - | ns |
| | | 10 | 40 | - | - | - | - | - | ns |
| Minimum $\overline{\text{MWR}}$ Pulse Width | t_{MWR} | 5 | 130 | - | - | 130 | - | - | ns |
| | | 10 | 60 | - | - | - | - | - | ns |
| Minimum $\overline{\text{IRX}}$ Pulse Width | t_{IRX} | 5 | 130 | - | - | 130 | - | - | ns |
| | | 10 | 60 | - | - | - | - | - | ns |

NOTE:

1. Typical values are for $T_A = 25^\circ\text{C}$ and $V_{DD} \pm 5\%$.

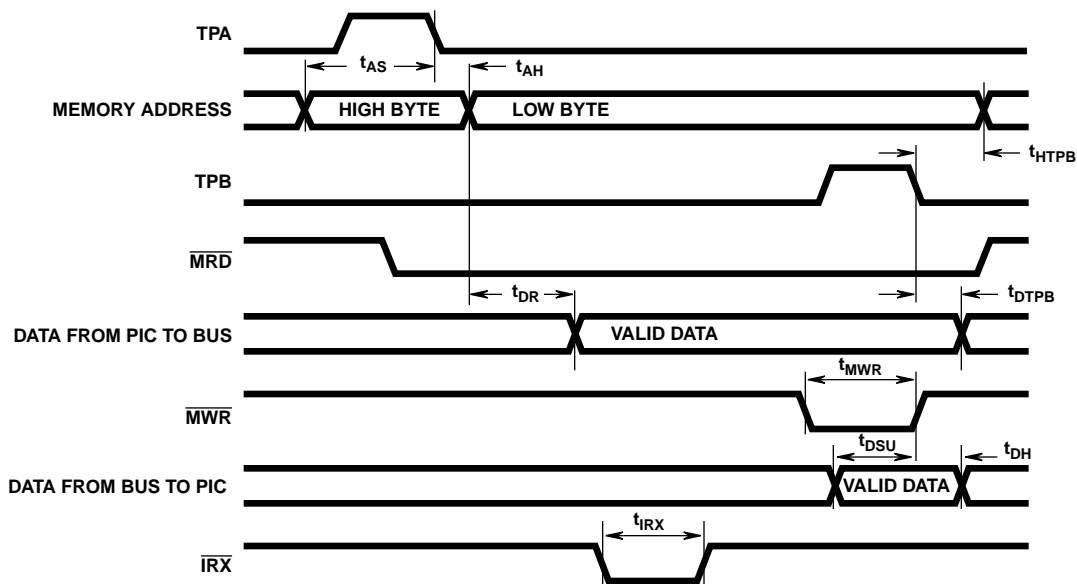


FIGURE 4. TIMING WAVEFORMS FOR CDP1877