

Am2833/2533

1024-Bit Static Shift Registers

Distinctive Characteristics

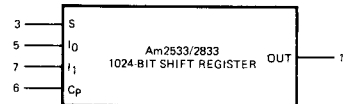
- Second source to Signetics 2533
- All inputs are low-level DTL/TTL compatible
- Static operation with single clock input.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- DC to 2.0MHz operation with Am2833

FUNCTIONAL DESCRIPTION

The Am2533/2833 is a quasi-static 1024-bit MOS shift register using low-threshold P-channel silicon gate technology.

The device has a single TTL/DTL compatible clock input, Cp. Data in the register is stored in static, cross-coupled latches while the clock is LOW, so that the clock may be stopped indefinitely in the LOW state. When the clock shifts from LOW to HIGH to LOW a dynamic transfer of data occurs from one static latch to the next. The input of the register is a two-input multiplexer with both data inputs available. A select line, S, determines whether data will be accepted from the I0 input (S = LOW) or the I1 input (S = HIGH). The register can be placed in the recirculate mode by tying the output, O, to one of the data inputs, and using the select line as a write/recirculate control. The Am2833 is functionally identical to the Am2533 but has superior performance over an extended temperature range.

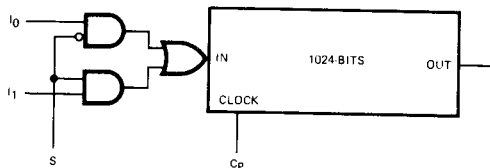
LOGIC SYMBOL



VCC = Pin 8
VGG = Pin 2
VDD = Pin 4

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LOGIC DIAGRAM

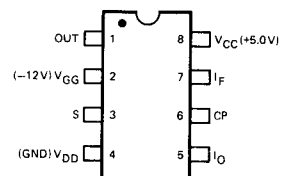


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ORDERING INFORMATION

| Package Type | Temperature Range | Am2533 Order Number | Am2833 Order Number |
|--------------|-------------------|---------------------|---------------------|
| Molded DIP | 0°C to +70°C | AM2533V | AM2833PC |
| Hermetic DIP | 0°C to +70°C | AM2533DC | AM2833DC |
| Hermetic DIP | -55°C to +125°C | | AM2833DM |

CONNECTION DIAGRAM Top View



Note: Pin 1 marked for orientation

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MAXIMUM RATING (Above which the useful life may be impaired)

| | |
|----------------------------------|---|
| Storage Temperature | -65°C to +150°C |
| Temperature (Ambient) Under Bias | -55°C to +125°C |
| V _{DD} Supply Voltage | V _{CC} -20V to V _{CC} +0.3V |
| V _{GG} Supply Voltage | V _{CC} -20V to V _{CC} +0.3V |
| DC Input Voltage | V _{CC} -20V to V _{CC} +0.3V |

OPERATING RANGE

| Part No. | Temperature | V _{CC} | V _{GG} | V _{DD} |
|--|-----------------|-----------------|-----------------|-----------------|
| Am2833PC/Am2533PC Am2833DC/Am2533DC | 0°C to +70°C | 5.0V ±5% | -12V ±5% | 0V |
| Am2833DM | -55°C to +125°C | 5.0V ±5% | -12V ±5% | 0V |

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|--------------------|--|--|--------------------------------|----------------------|----------------------|-------|
| V _{OH} | Output HIGH Voltage | V _{CC} = MIN., I _{OH} = -100μA | 2.4 | 3.5 | | Volts |
| V _{OL} | Output LOW Voltage | V _{CC} = MIN., I _{OL} = 1.6mA | | 0.2 | 0.4 | Volts |
| V _{IH} | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | V _{CC} -1 (Note 3) | | V _{CC} +0.3 | Volts |
| V _{IL} | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | V _{GG} | | 0.8 | Volts |
| I _{IL} | Input LOW Current | V _{CC} = MAX., V _{IN} = 0V, T _A = 25°C | | 10 | 500 | nA |
| I _{IH} | Input HIGH Current | T _A = 25°C, V _{IN} = V _{CC} -1.0 (Note 3) | -150 | -300 | | μA |
| I _{IT} | Peak input transition current (Note 3) | 1.5 ≤ V _{SS} - V _{IN} ≤ 4.0, T _A = 25°C | | | -1.6 | mA |
| V _I max | Voltage at maximum input current | T _A = 25°C | V _{SS} -4.0 | V _{SS} -3.0 | V _{SS} -1.5 | V |
| I _{CC} | V _{CC} Power Supply Current | f = 1.5MHz | Am2533 | 16 | 30 | mA |
| | | f = 2.0MHz | Am2833PC, DC | 16 | 54 | |
| | | | Am2833DM | 20 | 70 | |
| I _{GG} | V _{GG} Power Supply Current | f = 1.5MHz | Am2533 | -5.0 | -7.5 | mA |
| | | f = 2.0MHz | Am2833PC, DC | -5.0 | -14 | |
| | | | Am2833DM | -7.0 | -18 | |

Notes: 1. Typical limits are at V_{CC} = 5.0V, V_{GG} = -12V, 25°C ambient.

2. Power supply currents are with inputs and outputs open.

3. A special input pull-up circuit becomes active at V_{IN} = V_{SS} -3.5V to pull the internal input node up to the MOS threshold. To return the internal node to the LOW state, current must be drawn from the MOS input. This current is maximum at approximately 2.0V.

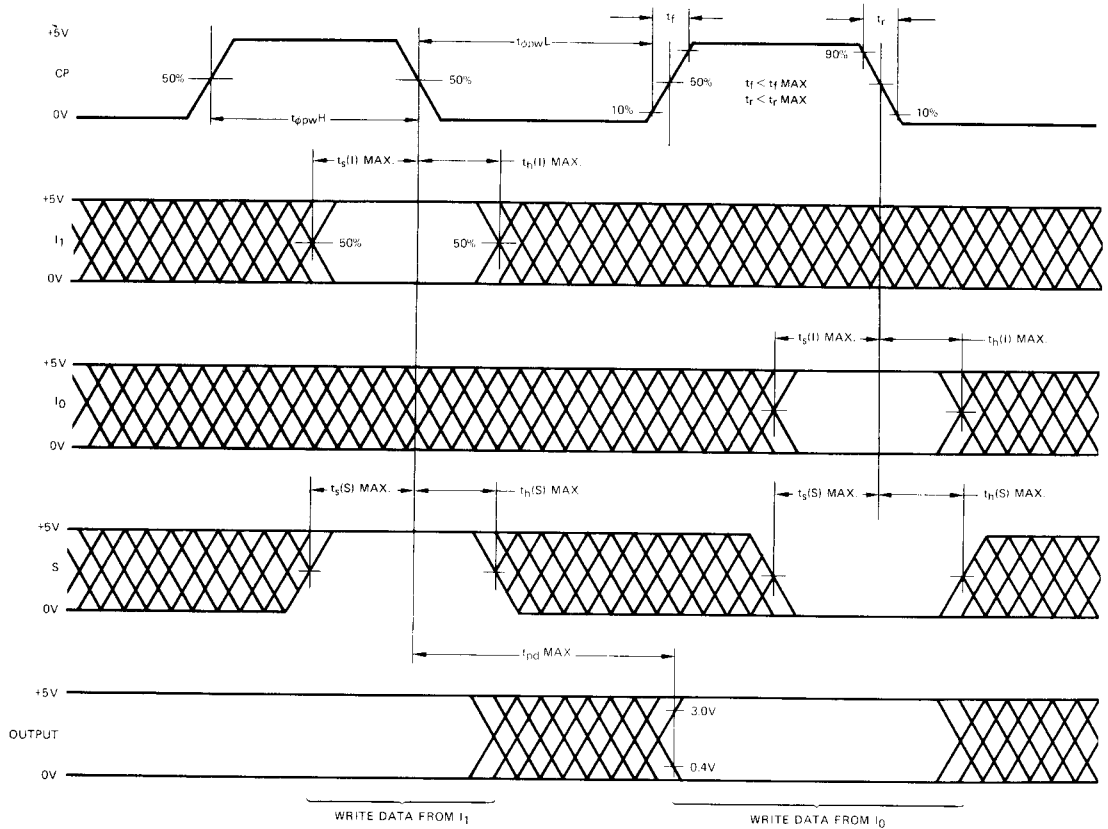
SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | Am2533 | | Am2833 | | Units |
|-----------------------------------|--|--|------------------|------|------------------|------|-------|
| | | | Min. (Note 1) | Max. | Min. (Note 1) | Max. | |
| f _{max} | Maximum Clock Frequency | | 1.5 | 2.0 | 2.0 | 3.0 | MHz |
| t _{φpwL} | Clock LOW Time | | 0.250 | ∞ | 0.200 | ∞ | μs |
| t _{φpwH} | Clock HIGH Time | | 0.350 | 100 | 0.250 | 100 | μs |
| t _r , t _f | Clock Rise and Fall Times | | | 1 | | 1 | μs |
| t _{s(L)} | Set-up Time, I _Q or I ₁ Input (see definitions) | t _r = t _f ≤ 25ns | 50 | | 50 | | ns |
| t _{h(L)} | Hold Time, I _Q or I ₁ Input (see definitions) | | 50 | | 50 | | ns |
| t _{s(S)} | Set-up Time, S Input (see definitions) | | 80 | | 80 | | ns |
| t _{h(S)} | Hold Time, S Input (see definitions) | | 50 | | 50 | | ns |
| t _{pd} | Delay, Clock to Output LOW or HIGH | R _L = 2.9k, C _L = 20pF | | 300 | | 300 | ns |
| t _{pr} , t _{pf} | Output Rise and Fall Times | 10% to 90% | | 150 | | 150 | ns |
| C _{in} | Capacitance, Any Input (Note 2) | f = 1MHz, V _{IN} = V _{CC} | | 3 | | 5 | pF |

Notes: 1. Typical limits are at V_{CC} = 5.0V, V_{GG} = -12.0V and T_A = 25°C

2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

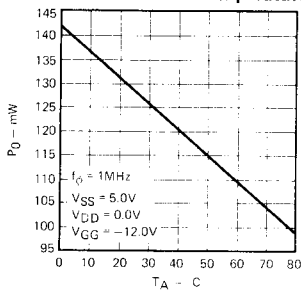
TIMING DIAGRAM



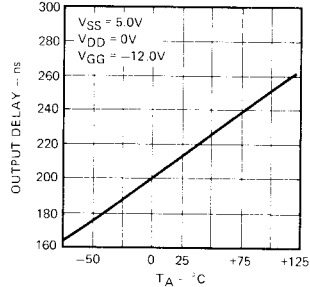
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TYPICAL PERFORMANCE CURVES

Power Dissipation Versus Ambient Temperature



t_{pd} as a Function of Ambient Temperature



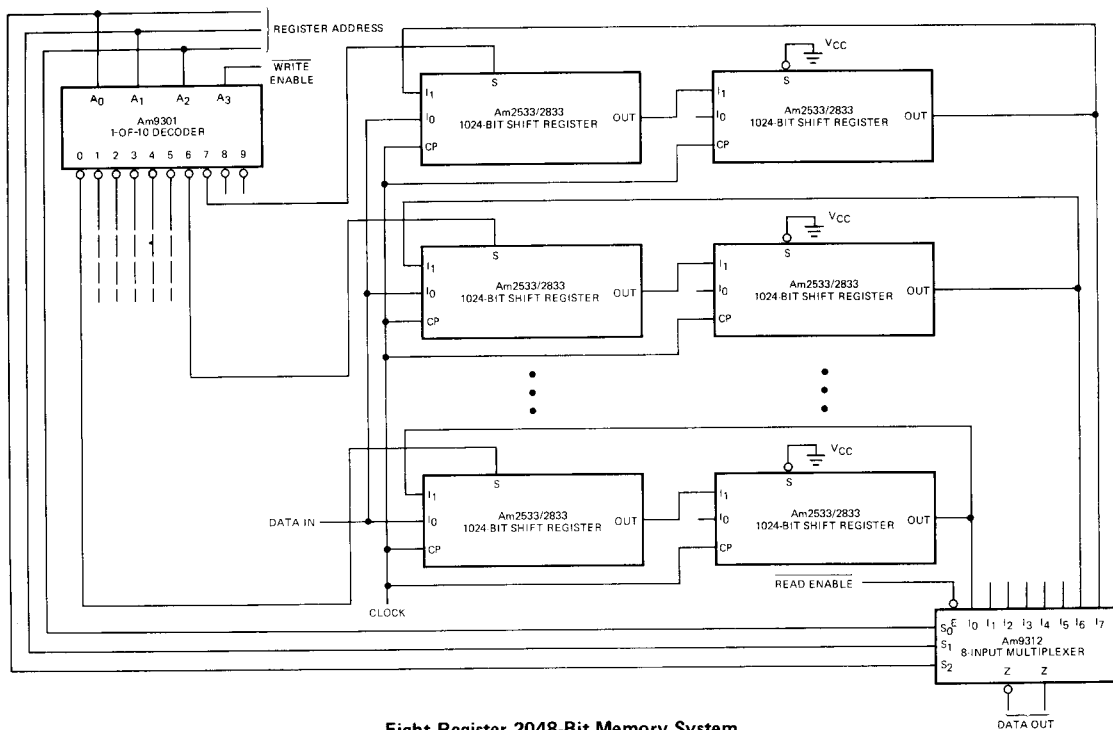
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DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

APPLICATIONS



Eight Register 2048-Bit Memory System

Data enters one of the eight 2048-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same.

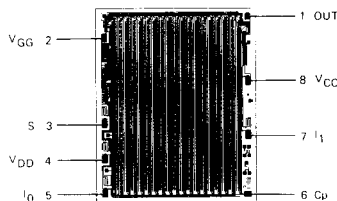
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TRUTH TABLE

| S | I ₀ | I ₁ | Data Entered |
|---|----------------|----------------|--------------|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

H = HIGH Voltage level
 L = LOW Voltage Level
 X = Don't Care

Metallization and Pad Layout



DIE SIZE: 0.133" X 0.163"

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