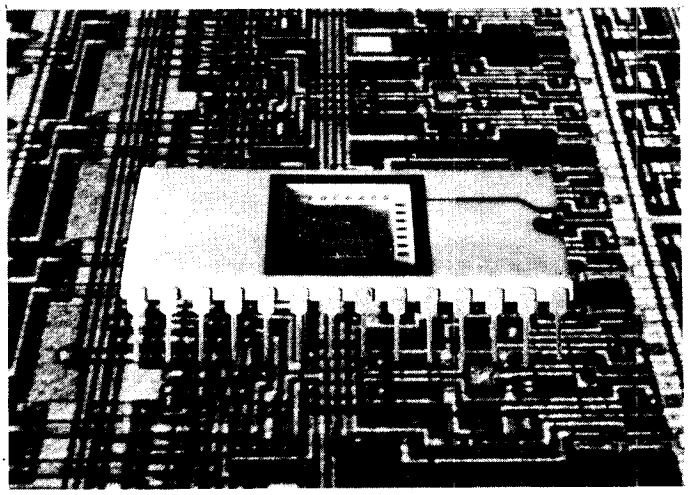
Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

AD574

PRELIMINARY TECHNICAL DATA

FEATURES

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8 or 16-Bit Microprocessor Bus Interface
- Guaranteed Linearity Over Temperature
  - 0 to 70°C – AD574J, K, L
  - -55°C to +125°C – AD574S, T, U
- No Missing Codes Over Temperature
- Fast Successive Approximation Conversion - 25μs
- Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10ppm/°C max AD574L, 12.5ppm/°C max AD574U
- Low Profile 28-Pin Ceramic DIP
- Low Power: 455mW
- Low Cost



PRODUCT DESCRIPTION

The AD574 is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8-12- or 16-bit microprocessor bus. The AD574 design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost.

One chip is the high performance AD565 12-bit DAC and voltage reference. It contains the high speed current output switching circuitry, laser-trimmed thin film resistor network, low T.C. buried zener reference and the precision input scaling and bipolar offset resistors. This chip is laser-trimmed at the wafer stage (LWT) to adjust ladder network linearity, voltage reference tolerance and temperature coefficient, and the calibration accuracy of input scaling and bipolar offset resistors.

The second chip uses the newly-developed LCI (linear-compatible integrated injection logic) process to provide the low-power I^2L successive-approximation register, converter control circuitry, clock, bus interface, and the high performance latching comparator. The precision, low-drift comparator is adjusted for initial input offset error at the wafer stage by the "zener-zap" technique which trims the comparator input stage to 1/10 LSB typical error. This form of trimming, while cumbersome for complex ladder networks, is an attractive alternative to thin film resistor trimming for a simple offset adjustment and eliminates the need for thin film processing for this portion of the circuitry.

The AD574 is available in six different grades. The AD574J, K, and L grades are specified for operation over the 0 to +70°C temperature range. The AD574S, T, and U are specified for the -55°C to +125°C range. All grades are packaged in a low-profile, 0.600 inch wide, 28-pin hermetically-sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD574 interfaces to most popular microprocessors with an 8-, 12-, or 16-bit bus without external buffers or peripheral interface controllers. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12-bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros.)
2. The AD574 will also operate equally well in a self-cycling, stand alone mode and can perform conversions and latch data into an external latch at a 40kHz sample rate.
3. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges, 0 to +10 and 0 to +20 volts unipolar, or -5 to +5 and -10 to +10 volts bipolar. Typical bipolar offset and full scale calibration of ±0.05% can be trimmed to zero with one external component each.
4. The internal buried zener reference is trimmed to 10.00 volts with a 1% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 1.5mA beyond that required for the reference and bipolar offset resistors.
5. The two-chip construction renders the AD574 inherently more reliable than hybrid multi-chip designs. All three military grades have guaranteed linearity error over the full -55°C to +125°C and are especially recommended for high performance needs in harsh environments. These units are available fully processed to MIL-STD-883B, Level B.

SPECIFICATIONS (typical @ +25°C with V_{CC} = +15, V_{LOGIC} = +5V, V_{DD} = -15V, unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	AD574J	AD574K	AD574L	UNITS
RESOLUTION (max)	12	12	12	Bits
NONLINEARITY ERROR				
25°C (max)	±1	±1/2	±1/2	LSB
T_{min} to T_{max} (max)	±1	±1/2	±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
UNIPOLAR OFFSET (max) (Adjustable to zero)	±2	±1	±1	LSB
BIPOLAR OFFSET (max) (Adjustable to zero)	±10	±4	±4	LSB
FULL SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero) 25°C (max)	0.3	0.2	0.2	% of F.S.
T_{min} to T_{max} (Without Initial Adjustment)	0.5	0.3	0.2	% of F.S.
(With Initial Adjustment)	0.22	0.12	0.05	% of F.S.
TEMPERATURE RANGE		0 to +70		°C
TEMPERATURE COEFFICIENTS (Using internal reference) Guaranteed max change T_{min} to T_{max}				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Gain	±9	±5	±2	LSB
	(50)	(27)	(10)	(ppm/°C)
POWER SUPPLY REJECTION Max change in Full Scale Calibration				
+13.5V ≤ V_{CC} ≤ +16.5V	±2	±1	±1	LSB
+4.5V ≤ V_{LOGIC} ≤ +5.5V	±1/2	±1/2	±1/2	LSB
-16.5V≤V_{DD}≤-13.5V	±2	±1	±1	LSB
ANALOG INPUTS				
Input Ranges				
Bipolar		-5 to +5		Volts
		-10 to +10		Volts
Unipolar		0 to +10		Volts
		0 to +20		Volts
Input Impedance				
10 Volt Span		5k (3k min, 7k max)		Ω
20 Volt Span		10k (6k min, 14k max)		Ω
POWER SUPPLIES				
Operating Range				
V_{LOGIC}		+4.5 to +5.5		Volts
V_{CC}		+13.5 to +16.5		Volts
V_{DD}		-13.5 to -16.5		Volts
Operating Current				
V_{LOGIC}		25 typ., 35 max		mA
V_{CC}		2 typ., 6 max		mA
V_{DD}		20 typ., 35 max		mA
POWER DISSIPATION		455 typ., 780 max		mW
INTERNAL REFERENCE VOLTAGE		10.00 ±0.1 (max)		Volts
Output Current (available for external loads)		1.5 min		mA

Specifications subject to change without notice.

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	AD574S	AD574T	AD574U	UNITS
RESOLUTION (max)	12	12	12	Bits
NONLINEARITY ERROR				
25°C (max)	±1	±1/2	±1/2	LSB
-25°C to +85°C (max)	±1	±1/2	±1/2	LSB
-55°C to +125°C (max)	±1	±1	±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
UNIPOLAR OFFSET (max) (Adjustable to zero)	±2	±1	±1	LSB
BIPOLAR OFFSET (max) (Adjustable to zero)	±10	±4	±4	LSB
FULL SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF IN to REF OUT) (Adjustable to zero) 25°C (max)	0.3	0.2	0.2	% of F.S.
T_{min} to T_{max} (Without Initial Adjustment)	0.8	0.6	0.3	% of F.S.
(With Initial Adjustment)	0.5	0.25	0.12	% of F.S.
TEMPERATURE RANGE	-55 to +125			°C
TEMPERATURE COEFFICIENTS (using internal reference) Guaranteed max change T_{min} to T_{max}				
Unipolar Offset	±2	±1	±1	LSB
	(5)	(2.5)	(2.5)	(ppm/°C)
Bipolar Offset	±4	±2	±1	LSB
	(10)	(5)	(2.5)	(ppm/°C)
Full Scale Calibration	±20	±10	±5	LSB
	(50)	(25)	(12.5)	(ppm/°C)
POWER SUPPLY REJECTION Max change in Full Scale Calibration				
$+13.5V \leqslant V_{CC} \leqslant +16.5V$	±2	±1	±1	LSB
$+4.5V \leqslant V_{LOGIC} \leqslant +5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V \leqslant V_{DD} \leqslant -13.5V$	±2	±1	±1	LSB
ANALOG INPUTS				
Input Ranges				
Bipolar		-5 to +5		Volts
		-10 to +10		Volts
Unipolar		0 to +10		Volts
		0 to +20		Volts
Input Impedance				
10 Volt Span		5k (3k min, 7k max)		Ω
20 Volt Span		10k (6k min, 14k max)		Ω
POWER SUPPLIES				
Operating Range				
V_{LOGIC}		+4.5 to +5.5		Volts
V_{CC}		+13.5 to +16.5		Volts
V_{DD}		-13.5 to -16.5		Volts
Operating Current				
V_{LOGIC}		25 typ., 35 max		mA
V_{CC}		2 typ., 6 max		mA
V_{DD}		20 typ., 35 max		mA
POWER DISSIPATION		455 typ., 780 max		mW
INTERNAL REFERENCE VOLTAGE		10.00 ±0.1 (max)		Volts
Output Current (available for external loads)		1.5 min		mA

Specifications subject to change without notice.

DIGITAL CHARACTERISTICS

ALL GRADES

(See Page 222S for Detailed Timing Specifications)

LOGIC INPUTS (Not including 12/$\overline{8}$, which must be hard-wired high or low.)

$4.5V \leqslant V_{LOGIC} \leqslant 5.5V$

Input Threshhold	
T_{min} to T_{max}	
Logic "1"	2.0 Volts min
Logic "0"	0.8 Volts max
Input Current	
T_{min} to T_{max}	
Logic "1"	10μA max
Logic "0"	10μA max

LOGIC OUTPUTS

T_{min} to T_{max}	
Bit Outputs and STS	
Output Sink Current	1.6mA min
(V_{OUT} = 0.4V max)	(1 TTL Load)
Output Source Current	
(V_{OUT} = 2.4V min)	0.5mA min
Output Leakage when Blanked	±40μA max

OUTPUT CODING

Unipolar	Positive True Binary
Bipolar	Positive True Offset Binary

CONVERSION TIME

	15μs min
	25μs typ
	35μs max

MINIMUM START PULSE WIDTH

AT CE (Pin 6) (Positive)	300ns
AT $\overline{CS}$ (Pin 3) (Negative)	400ns
AT R/$\overline{C}$ (Pin 5) (Negative)	400ns

ABSOLUTE MAXIMUM RATINGS

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common	0 to +16.5V
V_{DD} to Digital Common	0 to −16.5V
V_{LOGIC} to Digital Common	0 to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common	0 to V_{LOGIC}
Analog Inputs (REF, IN, BIP OFF, 10 V_{IN}) to Analog Common	±12V
20 V_{IN} to Analog Common	±24V
REF OUT	Indefinite short to common
	Momentary short to V_{CC}
Chip Temperature (J, K, L grades)	100°C
(S, T, U grades)	150°C
Power Dissipation	1000mW
Lead Temperature, Soldering	300°C, 10 sec.
Storage Temperature	−65°C to +150°C

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD574, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD574 is offered with 100% screening to MIL-STD-883B, method 5004.

Table I details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883B screening to these tests on a 100% basis.

TABLE I

TEST	METHOD
1) Internal Visual (Pre cap)	2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hours @ +150°C
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30kg
5) Seal, Fine and Gross	Method 1014, Test Condition A and C
6) Burn-in Test	Method 1015, Test Condition B, 168 hours @ +125°C
7) Final Electrical Tests	Performed 100% to all min and max specifications on data pages
8) External Visual	Method 2009

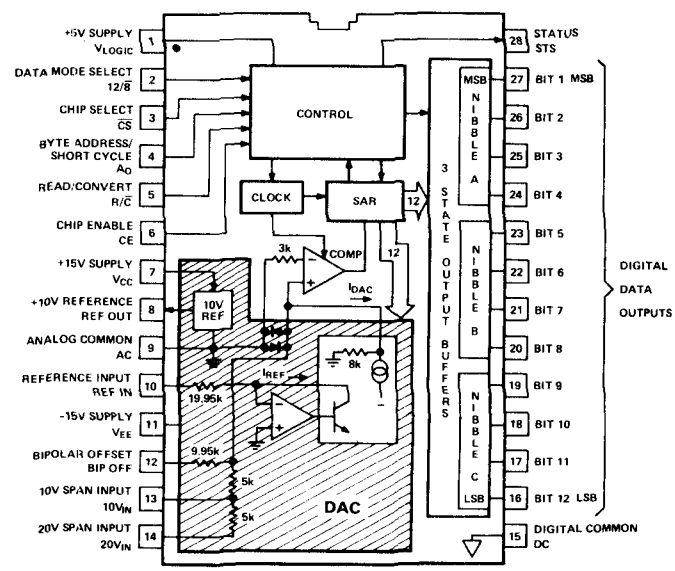


Figure 1. AD574 Block Diagram and Pin Configuration

THE AD574 OFFERS GUARANTEED MAXIMUM LINEARITY OVER THE FULL OPERATING TEMPERATURE RANGE

DEFINITIONS OF SPECIFICATIONS

NONLINEARITY ERROR

Nonlinearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 1/2LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The AD574K, L, T, and U grades are guaranteed for maximum nonlinearity error of ±1/2LSB over their respective temperature ranges. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The AD574J and S grades are guaranteed to ±1LSB max error over their respective temperature ranges. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. (In actual practice, our test systems limit minimum code width to 1/4LSB.) For the AD574K, L, T, and U grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD574J and S grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12 bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following two pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for 10,000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figure 5. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

POWER SUPPLY REJECTION

The standard specifications for the AD574 assume use of +5.00 and ±15.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

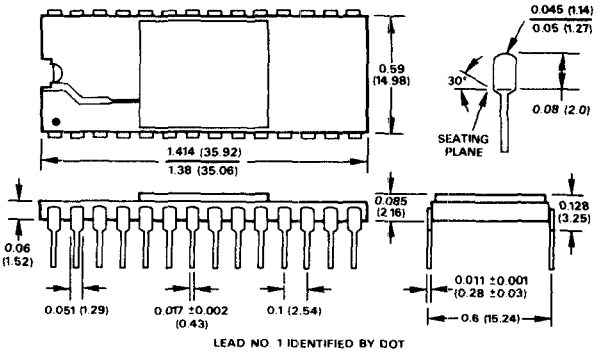


Figure 2. 28 Lead Dual-in-Line Package

AD574 ORDERING GUIDE

MODEL	TEMP RANGE	LINEARITY ERROR MAX (T_{min} to T_{max})	RESOLUTION NO MISSING CODES (T_{min} to T_{max})	FULL SCALE T.C. (ppm/°C)
AD574JD	0 to +70°C	±1LSB	11 Bits	50.0
AD574KD	0 to +70°C	±1/2LSB	12 Bits	27.0
AD574LD	0 to +70°C	±1/2LSB	12 Bits	10.0
AD574SD	-55 to +125°C	±1LSB	11 Bits	50.0
AD574TD	-25°C to +85°C	±1/2LSB		
	-55°C to +125°C	±1LSB	12 Bits	25.0
AD574UD	-25°C to +85°C	±1/2LSB		
	-55°C to +125°C	±1LSB	12 Bits	12.5

CIRCUIT OPERATION

The AD574 is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD574 is shown in Figure 3. The device consists of two chips, one containing the precision 12-bit DAC with voltage reference, the other containing the comparator, successive-approximation register, clock, output buffers and control circuitry.

When the control section is commanded to initiate a conversion (as described later), it then enables the clock and resets the successive-approximation register (SAR) to all zeros. (Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers). The SAR, timed by the clock, will then sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±1%; it is buffered and can supply up to 1.5mA to an external load in addition to that required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation. (Details of full scale and offset trimming are given on next page.)

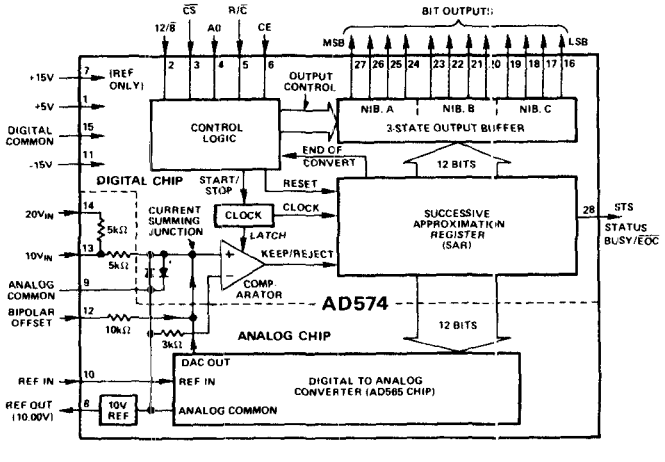


Figure 3. Block Diagram of AD574 12 bit A-to-D Converter

CONTROL FUNCTIONS

There are two sets of control pins on the AD574, the general control inputs (CE, $\overline{CS}$, and R/$\overline{C}$,) and the internal register control inputs (12/$\overline{8}$ and A_0). The general control pins function similarly to those on most A/D converters, performing device timing, addressing, cycle initiation and read enable functions. The internal register control inputs, which are not found on most A/D converters, select output data format and conversion cycle length.

The two major control functions, convert start and read enable, are controlled by CE, $\overline{CS}$, R/$\overline{C}$. Although all three inputs must be in the correct state to perform the function (for convert start, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 0; for read enable, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 1), the sequence does not matter. For large systems, typically microprocessor controlled, standard operation for convert start would be to first set R/$\overline{C}$ = 0 (from R/$\overline{W}$ line); address the chip with $\overline{CS}$ = 0, then apply a positive start pulse to CE. A read would be done similarly but with R/$\overline{C}$ = 1.

For a much simpler stand-alone operation, CE can be wired high, $\overline{CS}$ wired low, and R/$\overline{C}$ toggled as needed to initiate conversion. In this mode, a 200ns negative pulse will initiate conversion, and the data will automatically appear at the end of conversion. Alternatively, the R/$\overline{C}$ input can be brought low to start conversion, then brought high at any time later (after completion of conversion) to enable the data output lines. Many combinations of the above can be implemented by proper manipulation of the three control lines. Exact timing of these functions is shown on page 222S.

The A_0 (byte select) and 12/$\overline{8}$ (data format) inputs work together to control the output data and conversion cycle. In almost all situations 12/$\overline{8}$ is hard-wired high or low. If it is wired high, all 12 data lines will be enabled when the read function is called by the general control inputs. For an 8-bit bus interface, 12/$\overline{8}$ will be wired low. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at once, as addressed by A_0. For these applications, the 4LSB's (pins 16–19) should be hard-wired to the 4MSB's (pins 24–27). Thus, during a read, when A_0 is low the upper 8 bits are enabled and present data on pins 20 through 27. When A_0 goes high, the upper 8 data bits are disabled, the 4LSB's then present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 to 23.

The A_0 input performs an additional function of controlling conversion length. If A_0 is held low prior to cycle initiation, a full 12-bit cycle in about 25μs will result; if A_0 is held high prior to cycle initiation a shortened 8-bit cycle in about 16μs will result. The A_0 line must be set prior to cycle initiation and held in the desired position at least until STS goes high. Thus, for microprocessor interface applications, the A_0 line must be properly controlled during both the convert start and read functions.

The STS or status line goes high at the initiation of the conversion cycle and will go low when the cycle is complete.

UNIPOLAR RANGE CONNECTIONS FOR THE AD574

The AD574 contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +15, and -15 volts), the analog input, and the conversion initiation command, as discussed on next page. Analog input connections and calibration are easily accomplished; the unipolar operating mode is shown in Figure 4.

All of the thin film application resistors of the AD574 are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD574K guarantees ±1LSB max zero offset error and ±0.2% (8LSB) max full scale error. (Typical full scale error is ±2LSB.) If the offset trim is not required, pin 12 can be connected directly to pin 9; the two resistors and trimmer for pin 12 are then not needed. If the full scale trim is not needed, a 50Ω ±1% resistor should be connected between pin 8 and pin 10.

The analog input is connected between pin 13 and pin 9 for a 0 to +10V input range, between 14 and pin 9 for a 0 to +20V input range. The AD574 easily accommodates an input signal beyond the +15V supply. For the 10 volt span input, the LSB has a nominal value of 2.44mV, for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), the gain trimmer (R2) should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analog input to pin 13 (for a full scale range of 20.48V (5mV/bit), use a 500Ω trimmer into pin 14.) The gain trim described below is now done with these trimmers. The nominal input impedance into pin 13 is 5kΩ, and 10kΩ into pin 14.

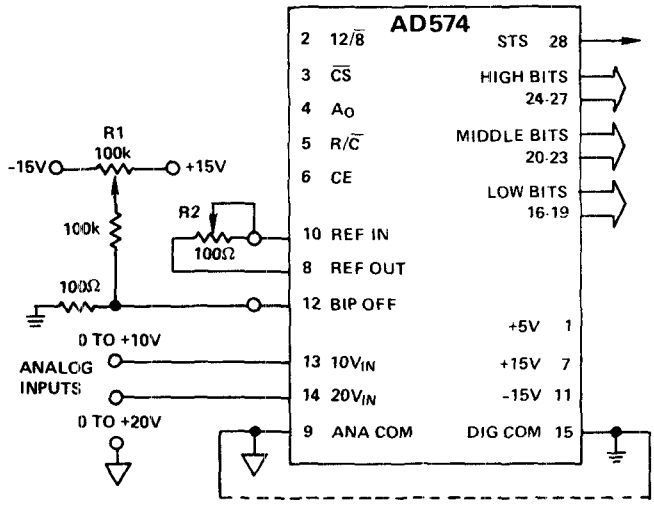


Figure 4. Unipolar Input Connections

UNIPOLAR CALIBRATION

The AD574 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range). If pin 12 is connected to pin 9, the unit typically will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±15mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963 for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 5. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2LSB above negative full scale (-4.9988V for the ±5V range) is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then, a signal is 1 1/2LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

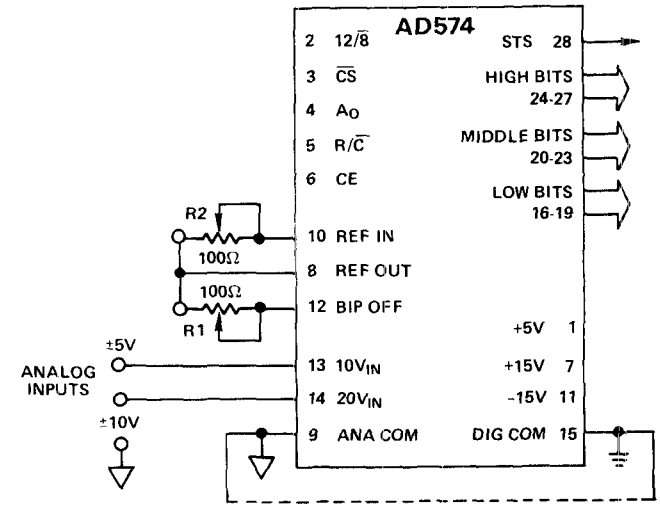


Figure 5. Bipolar Input Connections

The analog common at pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD574; it should be connected directly to the analog reference point of the system. The digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred. If digital common contains high frequency noise beyond 200mV, this noise may feed through the converter, so that some caution will be required in applying these grounds.

FULL CONTROL INTERFACE

The AD574 has a versatile set of control functions which will allow interface to a wide variety of microprocessor types as well as much simpler data acquisition systems, and even stand alone applications. It would be impossible to cover all of the potential AD574 control interface situations, but discussion of the two possible extreme situations and their timing will allow extension of the control concepts to most other applications.

STANDARD FULL CONTROL INTERFACE

The timing for the standard full control interface is shown in Figure 6. In this operating mode, $\overline{CS}$ is used as the address input which selects the particular device, R/$\overline{C}$ selects between the read data and start conversion functions, and CE is used to time the actual functions.

The left side of the figure shows the conversion start control. $\overline{CS}$ and R/$\overline{C}$ are brought low (their sequence does not matter), then the start pulse is applied to CE. The timing diagram shows a time delay for $\overline{CS}$ and R/$\overline{C}$ prior to the start pulse at CE. If less time than this is allowed, the conversion will still be started, but an appropriately longer pulse will be needed at CE. However, if the hold times for $\overline{CS}$ and R/$\overline{C}$ after the rising edge of the start pulse at CE are not followed, the conversion may not be initiated.

The A_0 line determines the conversion cycle length, and must be selected prior to conversion initiation. If A_0 is low, a 12-bit cycle results; if A_0 is high, an 8-bit short cycle results. Minimun set-up and hold times are shown. The status line goes high to indicate conversion in progress. The analog input signal is allowed to vary until the STS goes high. It must then be held steady until STS again goes low at the end of conversion.

The data read function operates in a similar fashion except that R/$\overline{C}$ is now held high. The data is stored in the output register and can be recalled at will until a new conversion cycle is commanded. In addition, if the converter is arranged in the 8-bit data mode, the A_0 line now functions as the byte select address, with set-up and hold times as shown. The A_0 line can be switched directly from one byte to the next without recycling the other three control lines. With A_0 low, pins 20 to 27 (bits 8–1) come out of three-state and present data. With A_0 high, pins 16–19 (bits 12–9) come out of three-state with data and pins 20–23 present active trailing zeros. In the 8-bit mode pins 16–19 will be hard-wired directly to pins 24–27 for direct two-byte loading onto an 8-bit bus. There are two delay times for the data lines after CE is brought low: t_{HD} is the delay until data is no longer valid; t_{HL} is the delay until the outputs are fully into the high impedance state.

TIMING SPECIFICATIONS – FULL CONTROL MODE

t_{DSC}	200ns max	t_{DD}	350ns max
t_{HEC}	300ns min	t_{HD}	100ns min
t_{SSC}	300ns min	t_{SSR}	250ns min
t_{HSC}	200ns min	t_{SRR}	0 min
t_{SRC}	200ns min	t_{SAR}	200ns min
t_{HRC}	200ns min	t_{HSR}	100ns min
t_{SAC}	0 min	t_{HRR}	0 min
t_{HAC}	300ns min	t_{HAR}	100ns min
t_C	15-35μs (12 bit) 10-20μs (8-bit)	t_{HL}	350ns max

TIMING FOR FULL CONTROL APPLICATIONS

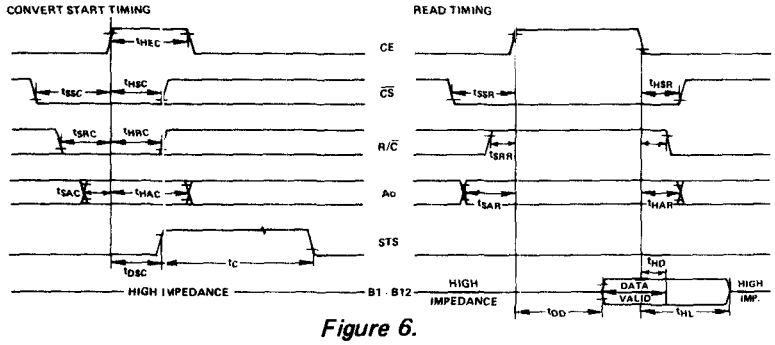


Figure 6.

STAND ALONE OPERATION

For simpler control functions, the AD574 can be controlled with just R/$\overline{C}$. In this case, CE is wired high, $\overline{CS}$ low, 12/$\overline{8}$ high, and A_0 low. There are two ways of cycling the device with this simple hook-up. If a negative pulse is used to initiate conversion as in Figure 7, the converter will automatically bring the 12 data lines out of three-state at the end of conversion. The data will remain valid on the output lines until another pulse is applied.

If the conversion is initiated by a high pulse as shown in Figure 8, the data lines are held in three-state at the end of conversion until R/$\overline{C}$ is brought high. The next conversion cycle is initiated when R/$\overline{C}$ goes low, the data from the previous cycle will remain valid for the time t_{HDR}. An alternative to the above is to toggle R/$\overline{C}$ as needed to initiate a new cycle on read data. Data will appear when R/$\overline{C}$ is brought high, a new cycle is initiated when R/$\overline{C}$ goes low.

TIMING SPECIFICATIONS – STAND ALONE MODE

t_{HRL}	400ns min	
t_{DS}	500ns max	
t_{HDR}	300ns min	
t_{HS}	-100ns min	+200ns max
t_{HRH}	150ns min	
t_{DDR}	350ns max	

t_C (12 bit convert) 15-35μs
t_C (8 bit convert) 10-20μs

TIMING FOR STAND ALONE OPERATIONS

SHORT LOW PULSE: OUTPUTS COME ON AFTER CONVERSION

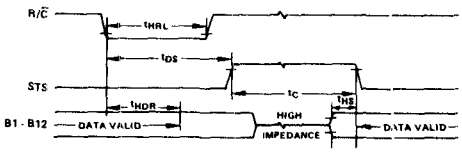


Figure 7.

SHORT HIGH PULSE: OUTPUTS SYNCHRONIZED TO RISING EDGE

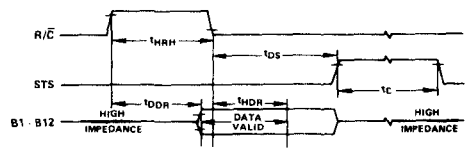


Figure 8.