LPTTL/SSI 9L00

LOW POWER QUAD 2-INPUT NAND GATE

DESCRIPTION — The low power TTL/SSI 9L00 consists of four NAND gates. Each gate has two inputs and performs positive logic. The 9L00 is designed for low power and medium speed operation.

- **TYPICAL PROPAGATION DELAY OF 20 ns**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 14-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

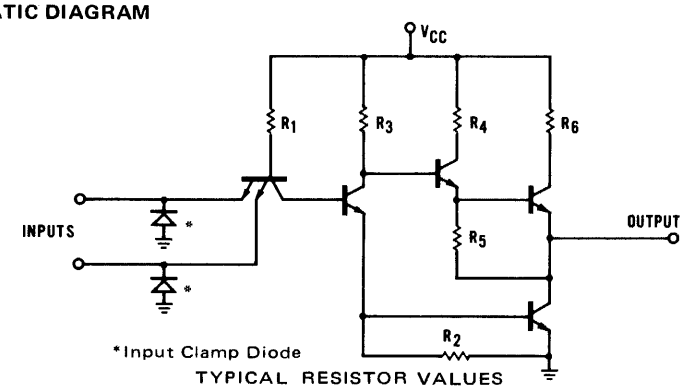
PIN NAMES

INPUTS (Pins 1, 2, 4, 5, 9, 10, 12, 13)
OUTPUTS (Pins 3, 6, 8, 11)

LOADING	
HIGH	LOW
0.5 U.L.	0.25 U.L.
10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

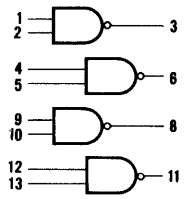
SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

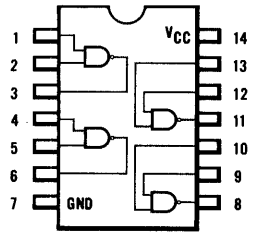
R_1 = 16 kΩ R_3 = 6 kΩ R_5 = 16 kΩ
R_2 = 5 kΩ R_4 = 600 Ω R_6 = 320 Ω

LOGIC SYMBOL

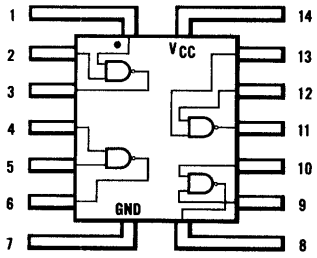


V_{CC} = PIN 14
GND = PIN 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9L00XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9L00XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted) (See Notes 1, 2)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. Note 3	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = V_{IL}	
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA, V_{IN} = V_{IH}	
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input LOW threshold voltage for all inputs	
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input HIGH threshold voltage for all inputs	
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V, Other Input = 4.5V	
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Other Input = 0.0V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{SC} (Note 4)	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V, Inputs Grounded	
I_{CC}	Power Supply Current		0.9	1.56	mA	V_{CC} = MAX., Inputs HIGH	
	per Gate		0.28	0.41	mA	V_{CC} = MAX., Inputs LOW	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
4. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH}	Turn Off Delay Input to Output		15		ns	V_{CC} = 5.0V See Fig. 1
t_{PHL}	Turn On Delay Input to Output		25		ns	C_L = 15 pF

SWITCHING TIME WAVEFORMS

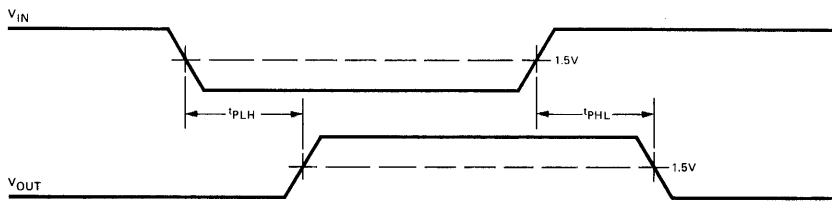


Fig. 1