

# DATA SHEET

**74F240/74F240A**

Octal inverter buffer (3-State)

**74F241/74F241A**

Octal buffer (3-State)

Product specification

1001 Jan 02

IC15 Data Handbook

## Buffers

## 74F240/74F240A/ 74F241/74F241A

### FEATURES

- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current
- Guaranteed output skew less than 2.0ns (74F240A/74F241A)
- Reduced ground bounce (74F240A/74F241A)
- Reduced  $I_{CC}$  (74F241A only)
- Reduced loading (74F240A  $I_{IL} = 100\mu\text{A}$ , 74F241A  $I_{IL} = 40\mu\text{A}$ )

### DESCRIPTION

The 74F240 and 74F241 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA. The device features two output enables, each controlling four of the 3-state outputs.

The 74F240A and 74F241A are functionally equivalent to their non-A counterparts. They have been designed to reduce effects of ground noise. Other advantages are noted in the features.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F240	4.3ns	37mA
74F240A	3.8ns	40mA
74F241	5.0ns	53mA
74F241A	4.5ns	32mA

### ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	
20-pin plastic DIP	N74F240N, N74F240AN, N74F241N, N74F241AN	SOT146-1
20-pin plastic SOL	N74F240D, N74F240AD, N74F241D, N74F241AD	SOT163-1
20-pin plastic SSOP II	N74F240DB	SOT339-1

### INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I <sub>an</sub> , I <sub>bn</sub>	Data inputs (74F240)	1.0/1.67	20 $\mu\text{A}$ /1.0mA
	Data inputs (74F240A)	1.0/0.167	20 $\mu\text{A}$ /100 $\mu\text{A}$
	Data inputs (74F241)	1.0/2.67	20 $\mu\text{A}$ /1.6mA
	Data inputs (74F241A)	1.0/0.067	20 $\mu\text{A}$ /40 $\mu\text{A}$
$\overline{\text{OE}}_a$ , $\overline{\text{OE}}_b$	Output enable inputs (active low) (74F240)	1.0/0.33	20 $\mu\text{A}$ /0.2mA
	Output enable inputs (active low) (74F240A)	1.0/0.167	20 $\mu\text{A}$ /100 $\mu\text{A}$
$\overline{\text{OE}}_a$ , OE <sub>b</sub>	Output enable input (74F241)	1.0/1.67	20 $\mu\text{A}$ /1.0mA
	Output enable input (74F241A)	1.0/0.067	20 $\mu\text{A}$ /40 $\mu\text{A}$
Y <sub>an</sub> , Y <sub>bn</sub>	Data outputs (74F241, 74F241A)	750/106.7	15mA/64mA
$\overline{\text{Y}}_a$ , $\overline{\text{Y}}_b$	Data outputs (74F240, 74F240A)	750/106.7	15mA/64mA

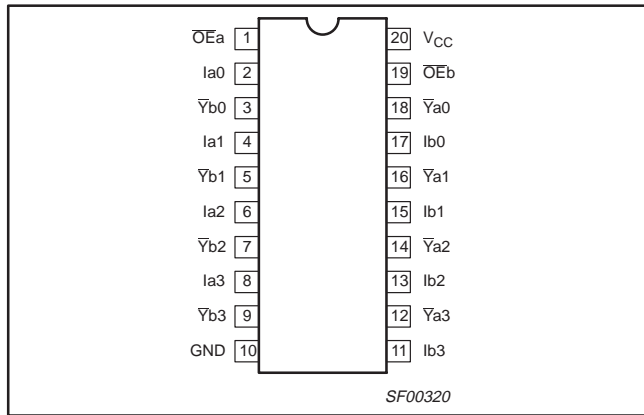
#### Note to input and output loading and fan out table

One (1.0) FAST unit load is defined as: 20 $\mu\text{A}$  in the high state and 0.6mA in the low state.

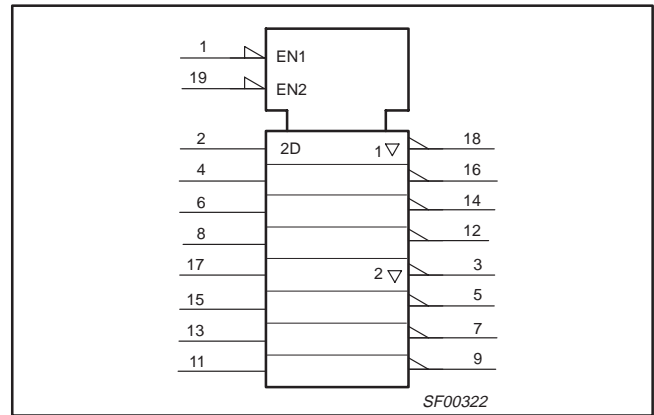
# Buffers

## 74F240/74F240A/ 74F241/74F241A

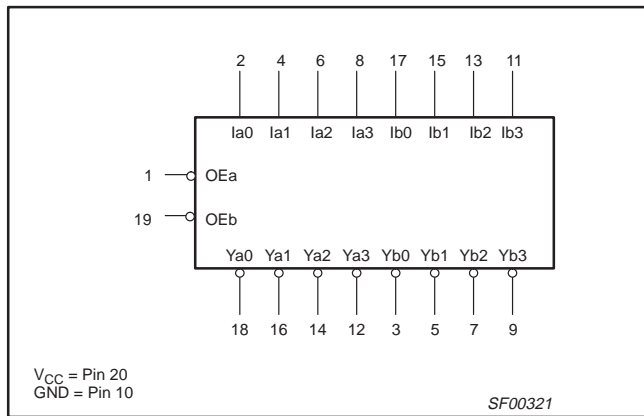
### PIN CONFIGURATION FOR 74F240/74F240A



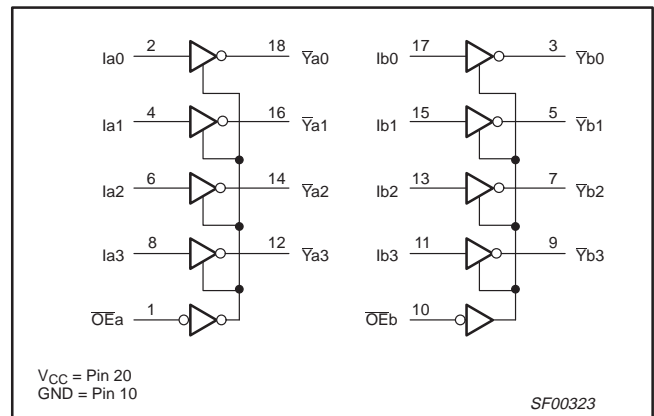
### IEC/IEEE SYMBOL FOR 74F240/74F240A



### LOGIC SYMBOL FOR 74F240/74F240A



### LOGIC DIAGRAM FOR 74F240/74F240A



### FUNCTION TABLE FOR 74F240/74F240A

INPUTS				OUTPUTS	
$\overline{OE}a$	$Ia$	$\overline{OE}b$	$Ib$	$\overline{Y}a$	$\overline{Y}b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

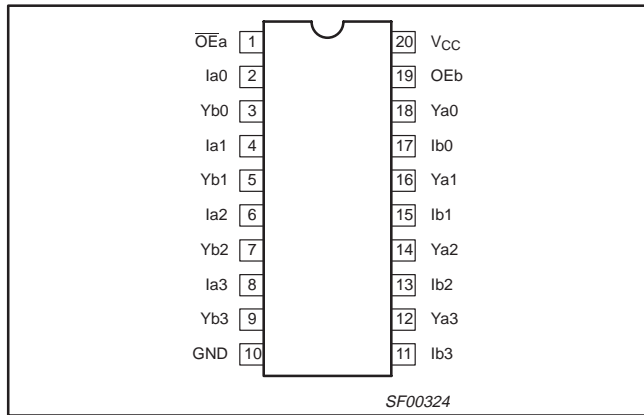
#### Notes to function table for 74F240/74F240A

- H = High voltage level
- L = Low voltage level
- X = Don't care
- Z = High impedance "off" state

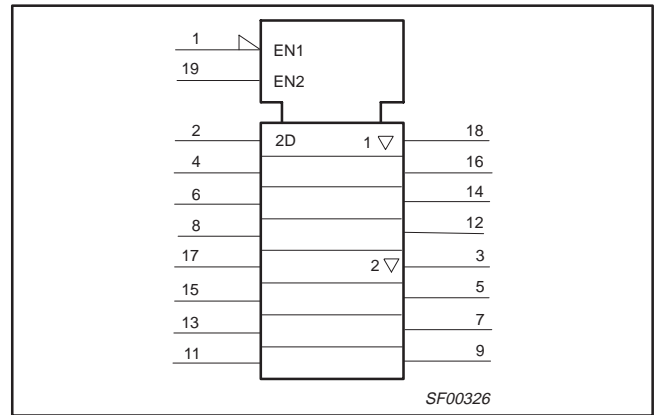
# Buffers

## 74F240/74F240A/ 74F241/74F241A

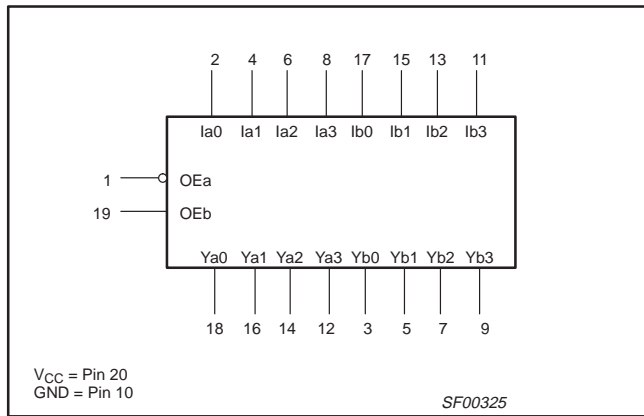
### PIN CONFIGURATION FOR 74F241/74F241A



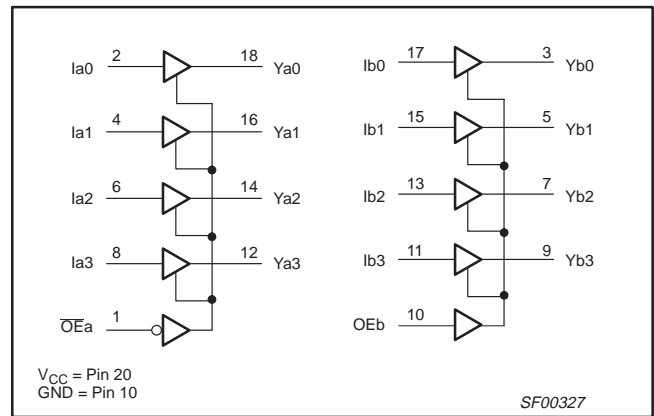
### IEC/IEEE SYMBOL FOR 74F241/74F241A



### LOGIC SYMBOL FOR 74F241/74F241A



### LOGIC DIAGRAM FOR 74F241/74F241A



### FUNCTION TABLE FOR 74F241/74F241A

INPUTS			OUTPUTS		
OEa	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

#### Notes to function table for 74F241/74F241A

- H = High voltage level
- L = Low voltage level
- X = Don't care
- Z = High impedance "off" state

## Buffers

74F240/74F240A/  
74F241/74F241A**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in high output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in low output state	128	mA
T <sub>amb</sub>	Operating free air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>Ik</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-15	mA
I <sub>OL</sub>	Low-level output current			64	mA
T <sub>amb</sub>	Operating free air temperature range	0		+70	°C

## Buffers

74F240/74F240A/  
74F241/74F241A

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>			LIMITS			UNIT	
						MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -3mA	±10%V <sub>C</sub>	2.4			V	
					±5%V <sub>CC</sub>	2.7	3.4		V	
			I <sub>OH</sub> = -15mA	±10%V <sub>C</sub>	2.0			V		
				±5%V <sub>CC</sub>	2.0			V		
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN,	I <sub>OL</sub> = MAX	±10%V <sub>C</sub>			0.50	V	
					±5%V <sub>CC</sub>		0.42	0.50	V	
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>				-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V					100	μA	
I <sub>IH</sub>	High-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V					20	μA	
I <sub>IL</sub>	Low-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			74F240 all inputs			-1.0	mA
						74F240A all inputs			-100	μA
						74F241 $\overline{OE}$ a, OEb			-1.0	mA
						74F241 I <sub>an</sub> , I <sub>bn</sub>			-1.6	mA
						74F241A all inputs			-40	μA
I <sub>OZH</sub>	Off-state output current, high-level voltage applied		V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V					50	μA	
I <sub>OZL</sub>	Off-state output current, low-level voltage applied		V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V					-50	μA	
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>		V <sub>CC</sub> = MAX			-100		-225	mA	
I <sub>CC</sub>	Supply current (total)		74F240	I <sub>CC</sub> H	V <sub>CC</sub> = MAX		12	18	mA	
				I <sub>CC</sub> L			50	70	mA	
				I <sub>CC</sub> Z			35	45	mA	
			74F240A	I <sub>CC</sub> H			28	37	mA	
				I <sub>CC</sub> L			58	75	mA	
				I <sub>CC</sub> Z			34	50	mA	
			74F241	I <sub>CC</sub> H		V <sub>CC</sub> = MAX		40	60	mA
				I <sub>CC</sub> L				60	90	mA
				I <sub>CC</sub> Z				65	90	mA
			74F241A	I <sub>CC</sub> H				20	30	mA
				I <sub>CC</sub> L				49	65	mA
				I <sub>CC</sub> Z				26	40	mA

## Notes to DC electrical characteristics

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

# Buffers

## 74F240/74F240A/ 74F241/74F241A

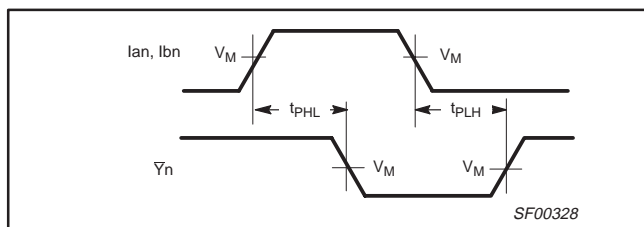
### AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT	
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>an</sub> , I <sub>bn</sub> to $\bar{Y}_n$	74F240	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 5.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to high or low level		Waveform 3 Waveform 4	3.0 4.5	5.0 6.5	7.5 8.5	3.0 4.0	9.0 10.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from high or low level		Waveform 3 Waveform 4	3.0 3.0	5.5 5.0	7.0 7.0	3.0 3.0	7.5 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>an</sub> , I <sub>bn</sub> to $\bar{Y}_n$	74F240A	Waveform 1	2.5 2.0	4.0 3.5	5.5 5.5	2.0 2.0	6.5 6.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to high or low level		Waveform 3 Waveform 4	2.0 3.5	4.0 5.0	6.5 7.5	2.0 3.0	7.0 8.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.5	3.5 2.5	6.0 5.0	1.5 1.0	6.5 5.5	ns
t <sub>sk(0)</sub>	Output skew <sup>1, 2</sup>		Waveform 5			1.5		2.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>an</sub> , I <sub>bn</sub> to Y <sub>n</sub>	74F241	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.2 6.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to high or low level		Waveform 3 Waveform 4	2.0 2.0	4.0 5.0	5.7 7.0	2.0 2.0	6.7 8.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>an</sub> , I <sub>bn</sub> to Y <sub>n</sub>	74F241A	Waveform 2	2.5 2.5	4.5 4.5	5.8 5.8	2.5 2.5	6.5 6.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to high or low level		Waveform 3 Waveform 4	2.5 3.5	4.5 5.0	6.0 7.0	2.0 3.0	6.7 8.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	6.0 5.5	1.5 1.0	6.5 6.0	ns
t <sub>sk(0)</sub>	Output skew <sup>1, 2</sup>		Waveform 5			1.5		2.0	ns

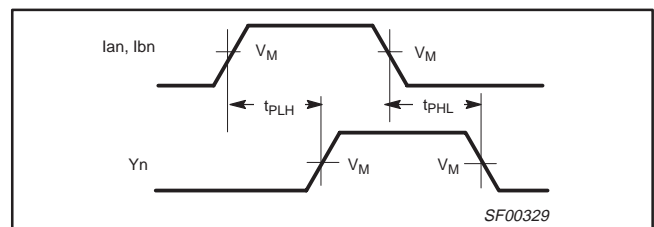
**Notes to AC electrical characteristics**

1. |t<sub>PN</sub> actual – t<sub>PM</sub> actual| for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V<sub>CC</sub>, loading, etc.,).

### AC WAVEFORMS



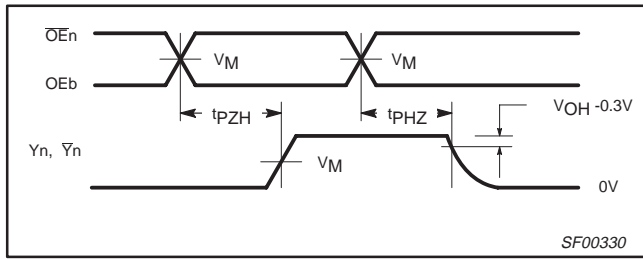
Waveform 1. Propagation delay for inverting outputs



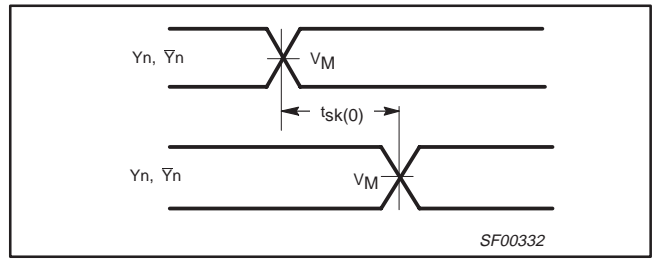
Waveform 2. Propagation delay for non-inverting outputs

# Buffers

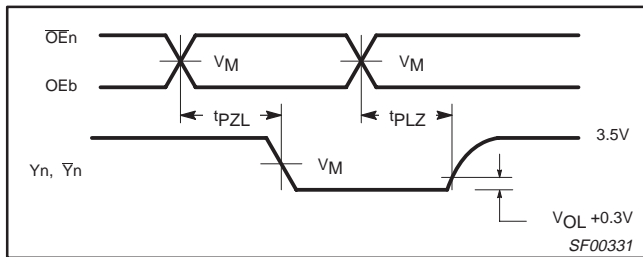
74F240/74F240A/  
74F241/74F241A



**Waveform 3. 3-state output enable time to high level and output disable time from high level**



**Waveform 5. Output skew**



**Waveform 4. 3-state output enable time to low level and output disable time from low level**

**Notes to AC waveforms**

1. For all waveforms,  $V_M = 1.5V$ .
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

**TEST CIRCUIT AND WAVEFORMS**

**Test Circuit for Open Collector Outputs**

**SWITCH POSITION**

TEST	SWITCH
$t_{pLZ}$	closed
$t_{pZL}$	closed
All other	open

**DEFINITIONS:**  
 $R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**Input Pulse Definition**

INPUT PULSE REQUIREMENTS						
family	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

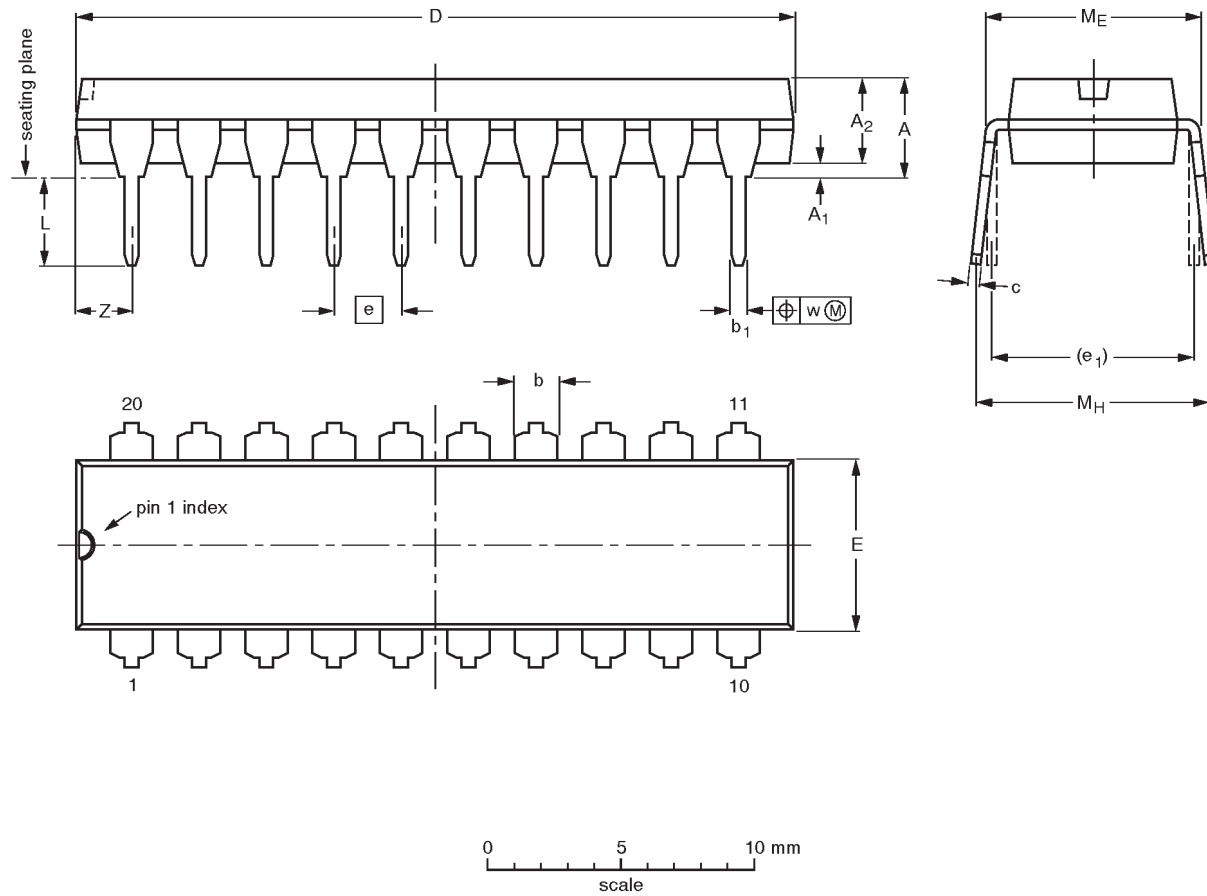


Buffers

74F240/74F240A  
74F241/74F241A

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

Buffers

74F240/74F240A  
74F241/74F241A

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	$\theta$
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

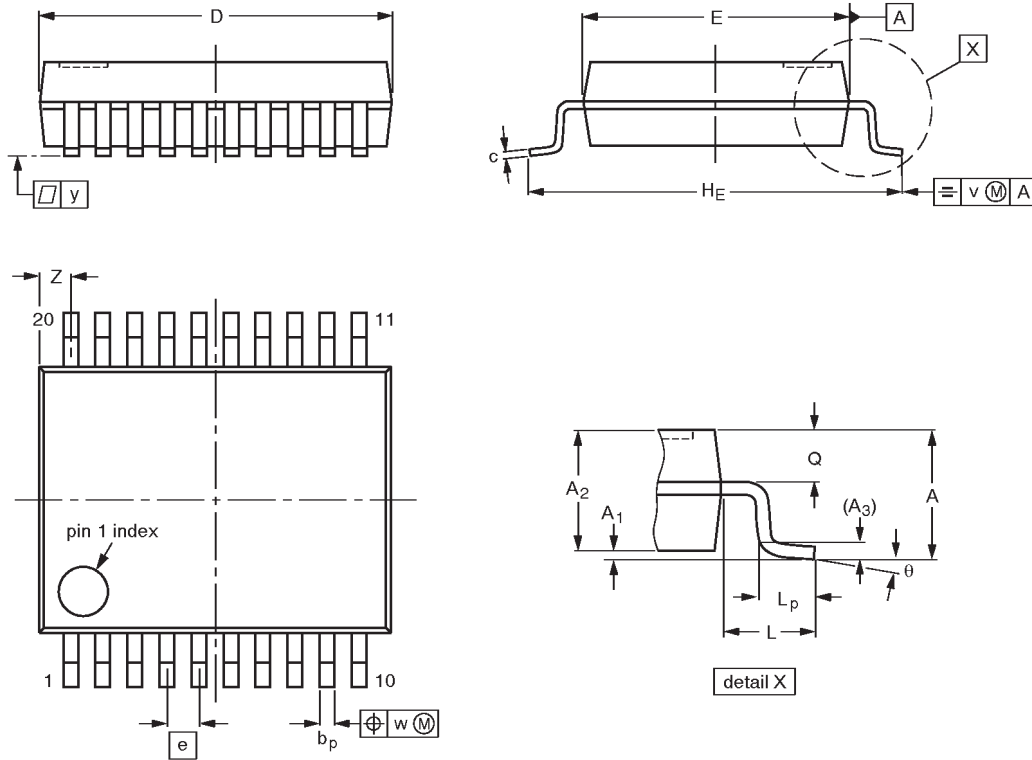
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

Buffers

74F240/74F240A  
74F241/74F241A

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

## Buffers

74F240/74F240A  
74F241/74F241A

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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print code

Date of release: 10-98

Document order number:

9397-750-05101

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