

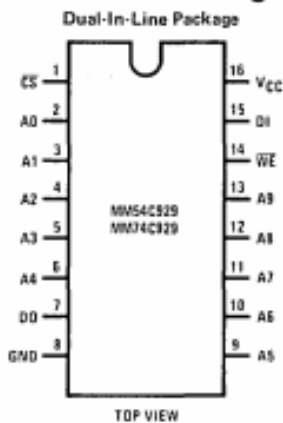
**MM54C929/MM74C929, MM54C930/MM74C930  
1024-Bit (1024 × 1) Static RAMs**
**General Description**

The MM54C929/MM74C929 and the MM54C930/MM74C930 1024 × 1 random access read/write memories are manufactured using silicon-gate CMOS technology. These RAMs are specifically designed to operate from standard 54/74 TTL power supplies; all inputs and outputs are TTL compatible. Data output is the same polarity as data input. Internal latches store the address inputs and data output. Chip select input  $\overline{CS1}$  serves as a chip strobe, controlling address and data latching. The Data-In and Data-Out terminals can be tied together for common I/O applications. Complete address decoding, 3-chip select functions (MM54C930/MM74C930) and TRI-STATE<sup>®</sup> output allow easy memory expansion and organization. The MM54C929/MM74C929 differs from the MM54C930/MM74C930 only in that  $\overline{CS1}$ ,  $\overline{CS2}$  and  $\overline{CS3}$  are internally connected together, providing a single chip-select input  $\overline{CS}$ .

Versatility, high speed, and low power make these RAMs ideal elements for use in many microprocessor, mini-computer and main-frame-memory applications.

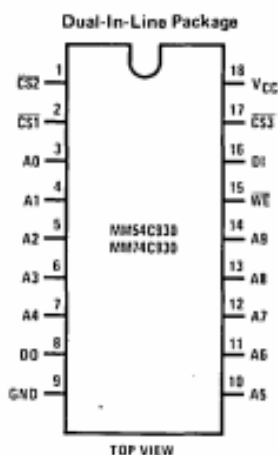
**Features**

- Fast access—250 ns max
- TRI-STATE outputs
- Low power—10  $\mu$ A max standby
- On-chip registers
- Single 5V supply
- Inputs and output TTL compatible
- Data retained with  $V_{CC}$  as low as 2V
- Can be operated common I/O

**Connection Diagrams**


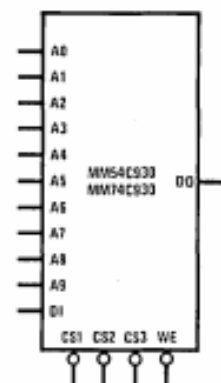
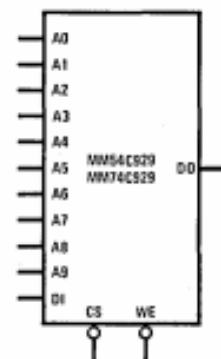
Order Number MM54C929J, MM74C929J  
or MM74C929J-3  
See NS Package J16A

Order Number MM74C929N or MM74C929N-3  
See NS Package N16A



Order Number MM54C930J, MM74C930J  
or MM74C930J-3  
See NS Package J18A

Order Number MM74C930N or MM74C930N-3  
See NS Package N18A

**Logic Symbols**


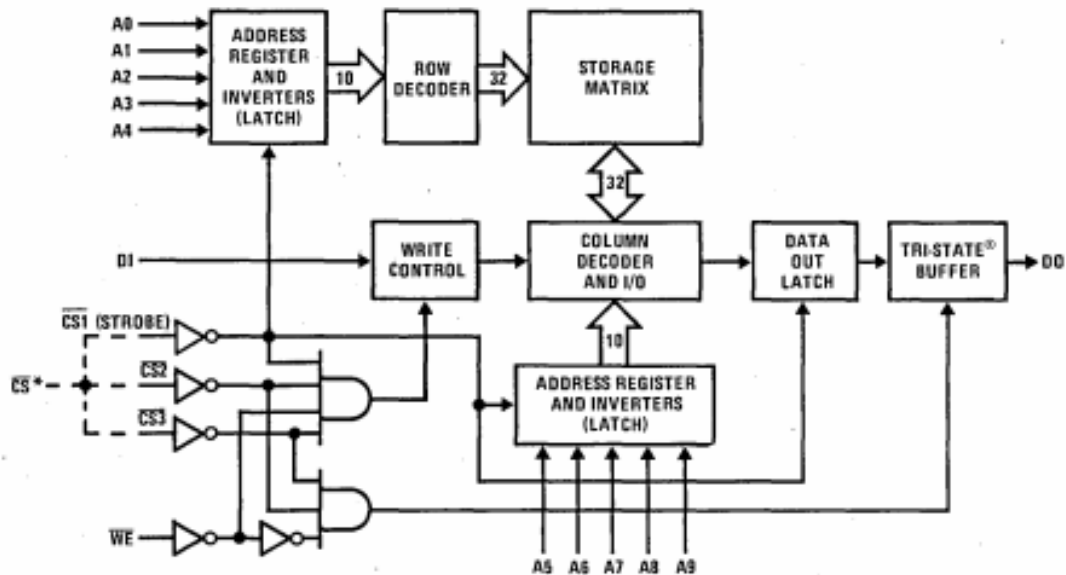
## Functional Description

Address inputs are clocked into the input latches by the falling edge of chip strobe  $\overline{CS1}$ ; set-up and hold times must be observed on these input signals (see timing diagram). The true and complement address information is fed to the row and column decoders which select one of the 1024-bit locations. The addressed bit is fed, via a sense amplifier, to the output register and TRI-STATE buffer. The information is latched into the output register on the rising edge of chip strobe  $\overline{CS1}$ . The output is in a high impedance state when the chip is not selected ( $\overline{CS2}$  or  $\overline{CS3}$  high) or when writing ( $\overline{WE}$  low). Output buffer control is independent of chip strobe  $\overline{CS1}$ .

## Reduced-Voltage Operation

These memories will retain data with reduced  $V_{CC}$  and hence are useful for battery-backup data storage. Certain precautions must be observed as  $V_{CC}$  is reduced: (1) input voltages must remain between the  $V_{CC}$  and ground of the RAM or supply latch-up can occur, (2) WRITE mode must be avoided, (3) during power-up of  $V_{CC}$ , strobe ( $\overline{CS}$  for the MM74C929 and  $\overline{CS1}$  for the MM74C930) logic state must be maintained (either GND or  $V_{CC}$ ) while address control lines stabilize.

## Logic Diagram \*



\*The MM74C930 has 3 chip selects  $\overline{CS1}$ ,  $\overline{CS2}$  and  $\overline{CS3}$ . The MM74C929 has these internally connected together providing a single chip select input  $\overline{CS}$ .

FIGURE 1

### Absolute Maximum Ratings

Supply Voltage, $V_{CC}$	7V
Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Storage Temperature Range	-65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering 10 seconds)	300°C

### Operating Conditions

Operating Temperature Range	MM54C929, MM54C930	-55°C to +125°C
	MM74C929, MM74C930	-40°C to +85°C
	MM74C929-3, MM74C930-3	0°C to +70°C

### DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ , $T_A =$ Operating Range, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MM54C929, MM54C930		MM74C929, MM74C930		MM74C929-3, MM74C930-3 (NOTE 1)		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
$V_{IH}$	Logical "1" Input Voltage		$V_{CC}-2.0$	$V_{CC}$	$V_{CC}-2.0$	$V_{CC}$	$V_{CC}-2.0$	$V_{CC}$	V
$V_{IL}$	Logical "0" Input Voltage		0	0.8	0	0.8	0	0.8	V
$V_{OH1}$	Logical "1" Output Voltage	$I_{OH} = 1 \text{ mA}$	2.4		2.4		2.4		V
$V_{OH2}$	Logical "1" Output Voltage	$I_{OUT} = 0$	$V_{CC}-0.1$		$V_{CC}-0.1$		$V_{CC}-0.1$		V
$V_{OL1}$	Logical "0" Output Voltage	$I_{OL} = 2.0 \text{ mA}$		0.4		0.4		0.4	V
$V_{OL2}$	Logical "0" Output Voltage	$I_{OUT} = 0$		0.01		0.01		0.01	V
$I_{IL}$	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	-1.0	1.0	-1.0	1.0	-1.0	1.0	$\mu\text{A}$
$I_O$	Output Leakage	$0V \leq V_O \leq V_{CC}$ , (Note 2)	-1.0	1.0	-1.0	1.0	-1.0	1.0	$\mu\text{A}$
$I_{CC}$	Supply Leakage Current	$V_{IN} = V_{CC}$ , $V_O = 0V$		20		10		100	$\mu\text{A}$
$V_{DR}$	$V_{CC}$ for Data Retention	(Note 3)	2.0		2.0		2.0		V
$I_{DR}$	$I_{CC}$ for Data Retention	$V_{CC} = 2V$ , $T_A = 25^\circ\text{C}$ , (Note 2)		0.01 (typ)		0.01 (typ)		0.1 (typ)	$\mu\text{A}$

Note 1:  $V_{CC} = 5V \pm 5\%$ .

Note 2:  $\overline{CS2} = \overline{CS3} = V_{CC}$  or  $\overline{CS} = V_{CC}$ .

Note 3:  $\overline{CS2}$  or  $\overline{CS3}$  or  $\overline{CS} = V_{CC} - 2V$  or  $-2V$ , whichever is greater.

### AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ , $T_A =$ Operating Range, unless otherwise noted

TTL Interface ( $V_{IH} = V_{CC} - 2V$ ,  $V_{IL} = 0.8V$ , Input  $t_{RISE} = t_{FALL} = 5 \text{ ns}$ , Load = 1 TTL Gate + 50 pF)

SYMBOL	PARAMETER	MM54C929, MM54C930		MM74C929, MM74C930		MM74C929-3, MM74C930-3 (NOTE 1)		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_C$	Cycle Time	290		255		330		ns
$t_{ACC}$	Access Time From Address		265		240		315	ns
$t_{ACS}, t_{ACS1}$	Access Time From $\overline{CS}$ , $\overline{CS1}$		250		225		300	ns
$t_{AS}$	Address Set-Up Time	15		15		15		ns
$t_{AH}$	Address Hold Time	50		50		50		ns
$t_{OE}$	Output Enable Time		150		130		130	ns
$t_{OD}$	Output Disable Time		150		130		130	ns
$t_{\overline{CS}}, t_{\overline{CS1}}$ (Note 4)	$\overline{CS}$ , $\overline{CS1}$ Pulse Width (Negative)	150		130		165		ns
$t_{CS}, t_{CS1}$	$\overline{CS}$ , $\overline{CS1}$ Pulse Width (Positive)	140		125		165		ns
$t_{WP}$	Write Pulse Width (Negative)	150		130		165		ns
$t_{DS}$	Data Set-Up Time, (Note 5)	150		140		140		ns
$t_{DH}$	Data Hold Time, (Note 5)	0		0		0		ns

Note 4: Greater than minimum  $\overline{CS}$  pulse width must be used when reading data from the MM54C929/MM74C929 to ensure that output TRI-STATING does not occur before data becomes valid. Writing has no such limitation.

Note 5:  $t_{DS}$  and  $t_{DH}$  are referenced to the low-to-high transition of  $\overline{CS1}$  or  $\overline{CS2}$  or  $\overline{CS3}$  or  $\overline{WE}$ , whichever switches first, for the MM54C930/MM74C930 and are referenced to the  $\overline{CS}$  or  $\overline{WE}$  low-to-high transition, whichever switches first, for the MM54C929/MM74C929.

## Capacitance (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
$C_{IN}$	Input Capacitance	$V_{IN} = 0, f = 1 \text{ MHz}, T_A = 25^\circ\text{C}$	4	7	pF
$C_O$	Output Capacitance	$V_{IN} = 0, f = 1 \text{ MHz}, T_A = 25^\circ\text{C}$	6	9	pF
$C_{\overline{CS}}$	Chip Select Capacitance	MM54C929/MM74C929, MM74C929-3	8	12	pF

Note 6: Capacitance maximum is guaranteed by periodic testing.

## Truth Tables

MM54C929/MM74C929

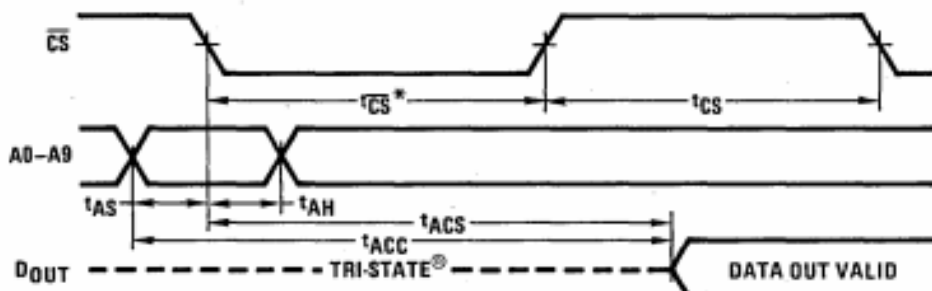
$\overline{CS}$	$\overline{WE}$	DI	FUNCTION
1	X	X	Output in Hi-Z State
X	0	X	Output in Hi-Z State
0	0	0	Write "0," Output in Hi-Z State
0	0	1	Write "1," Output in Hi-Z State
0	1	X	Read Data, Output Enabled

MM54C930/MM74C930

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{WE}$	DI	FUNCTION
X	1	X	X	X	Output in Hi-Z State
X	X	1	X	X	Output in Hi-Z State
X	X	X	0	X	Output in Hi-Z State
0	0	0	0	0	Write "0," Output in Hi-Z State
0	0	0	0	1	Write "1," Output in Hi-Z State
0	0	0	1	X	Read Data, Output Enabled

X = Don't care

## Switching Time Waveforms



\*Greater than minimum  $\overline{CS}$  pulse width must be used when reading data from the MM54C929/MM74C929 to ensure that output TRI-STATING does not occur before data becomes valid. Writing has no such limitation, (Figure 4a).

FIGURE 2a. MM54C929/MM74C929 Read Cycle

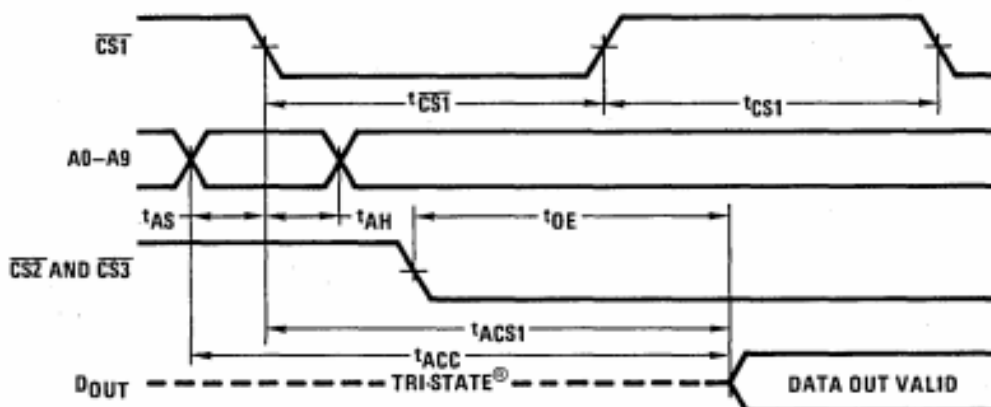
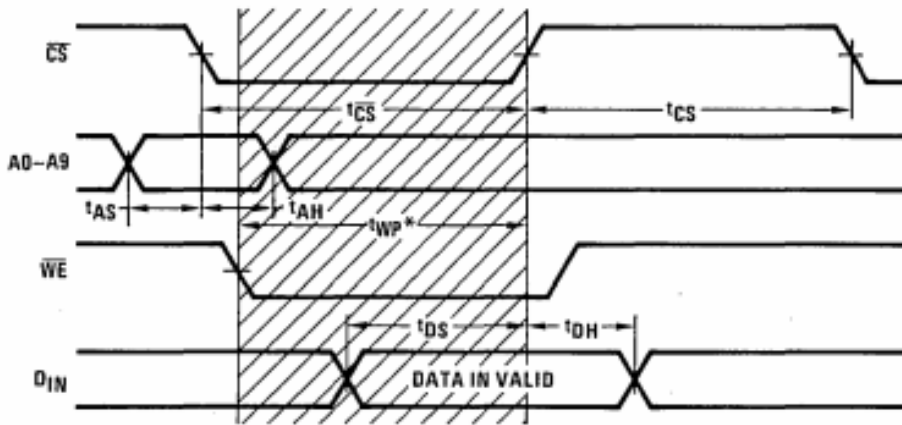


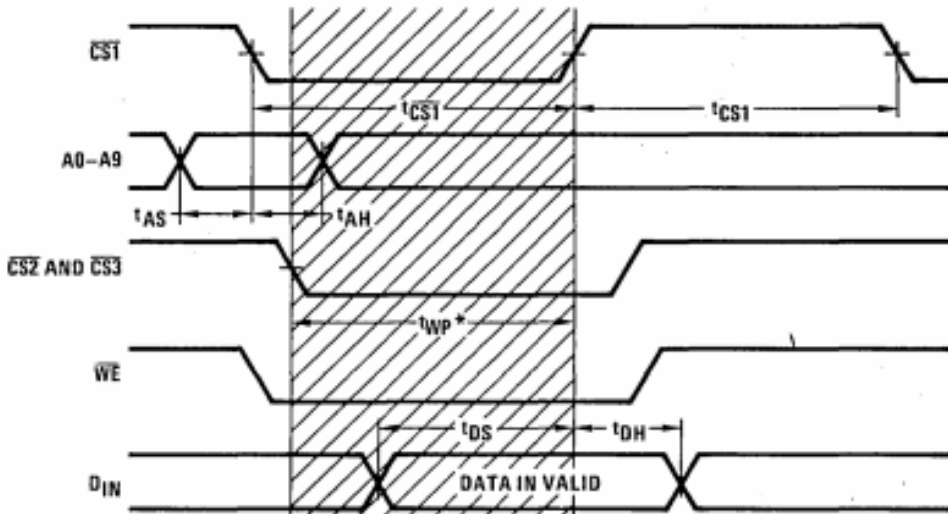
FIGURE 2b. MM54C930/MM74C930 Read Cycle

Switching Time Waveforms (Continued)



\*  $t_{WP}$  (the Write Pulse width) is the time  $\overline{CS}$  and  $\overline{WE}$  are coincidentally low

FIGURE 3a. MM54C929/MM74C929 Write Cycle



\*  $t_{WP}$  (the Write Pulse width) is the time  $\overline{CS1}$ ,  $\overline{CS2}$ ,  $\overline{CS3}$  and  $\overline{WE}$  are coincidentally low

FIGURE 3b. MM54C930/MM74C930 Write Cycle

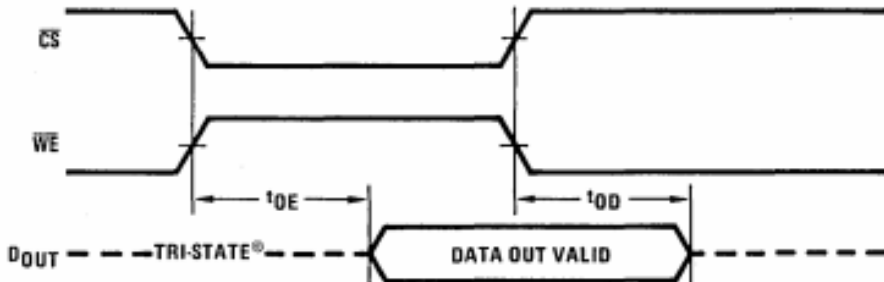


FIGURE 4a. MM54C929/MM74C929

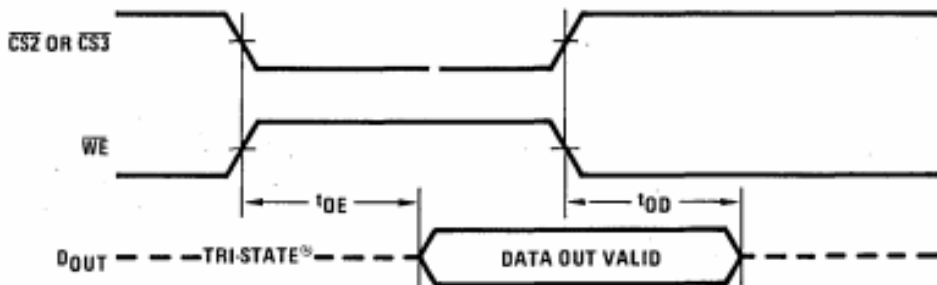
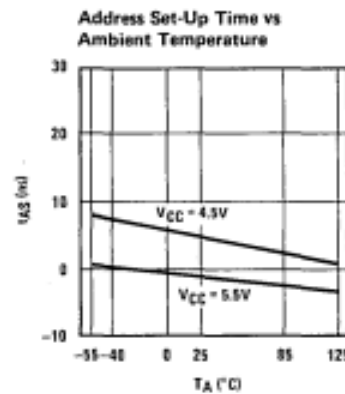
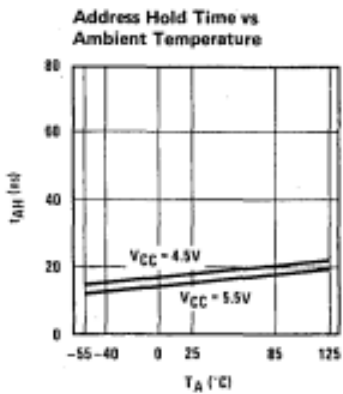
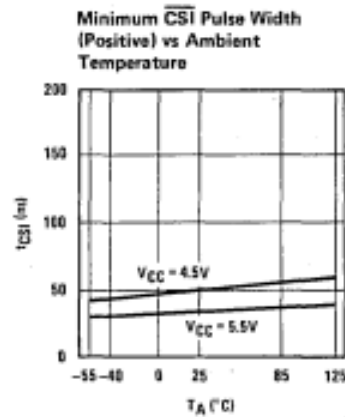
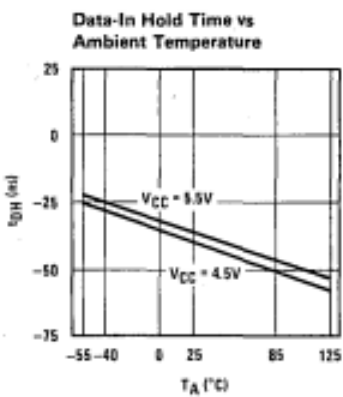
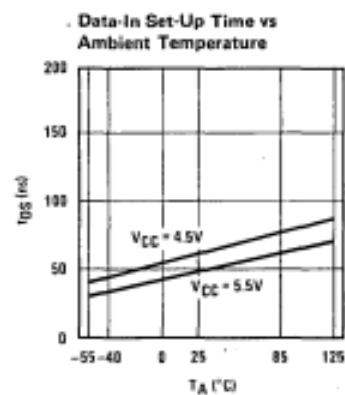
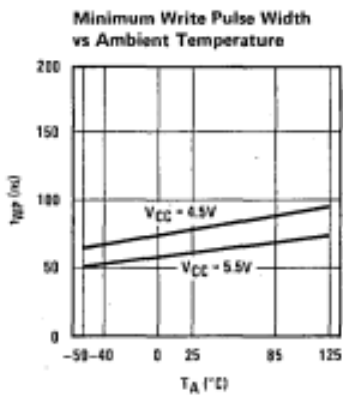
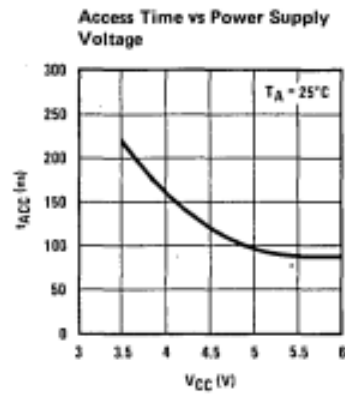
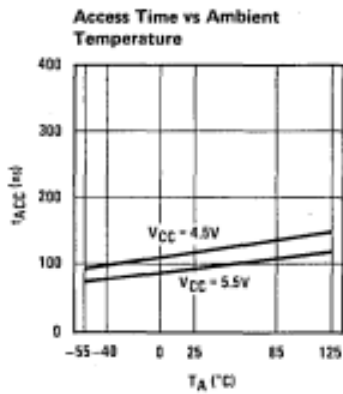


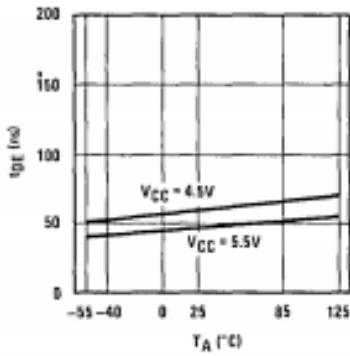
FIGURE 4b. MM54C930/MM74C930

## Typical Performance Characteristics

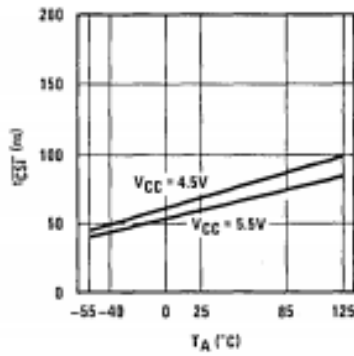


Typical Performance Characteristics (Continued)

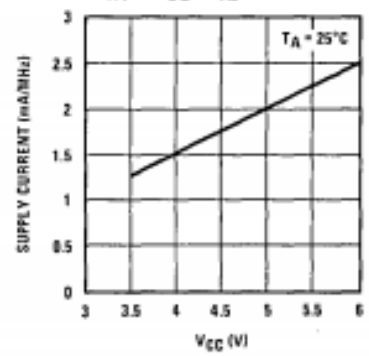
Output Enable Time vs Ambient Temperature



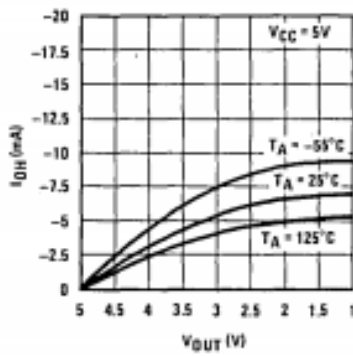
Minimum CS1 Pulse Width (Negative) vs Ambient Temperature



Dynamic Current vs Power Supply Voltage (VIH = VCC, VIL = 0V)



Output Source Current vs Output Voltage



Output Sink Current vs Output Voltage

